how to derive the appropriate frequency transformation in the digital domain from the corresponding ones in the analog domain via the bilinear z transform.

The procedure for the proposed digital realization is extended to the case of a 2-D digital filter realization. Starting with a doubly terminated LC ladder network in two variables, 2-D digital two-port realizations for some of the possible series and shunt elements of the ladder are derived which are canonic with respect to multipliers. An example of designing a circularly symmetric 2-D digital filter is considered, where a procedure is outlined as to how to go about choosing a particular network structure and then to obtain the element values using a known optimization procedure to approximate the ideal spatial frequency response.

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LIST OF ABBREVIATIONS AND SYMBOLS

LP	Lowpass
HP	Highpass
BP	Bandpass
BS	Bandstop
z	Complex variable in the digital domain
s	Complex variable in the analog domain
ω	Frequency variable in the analog domain
Ω	Frequency variable in the digital domain
T	Sampling period
$\tilde{N}$	Analog network
N	Digital 2-port
$\begin{bmatrix} \tilde{a}_i \\ \tilde{b}_i \end{bmatrix}$, $i=1,2$	Wave variables at ports 1 and 2 of an analog network
$\begin{bmatrix} a_i \\ b_i \end{bmatrix}$, $i=1,2$	Digital inputs and outputs at ports 1 and 2 of a digital 2-port
$\begin{bmatrix} \tilde{\mu} & \tilde{\lambda} \\ \tilde{\nu} & \tilde{K} \end{bmatrix} = [\tilde{F}]$	Wave or scattering matrix of an analog 2-port
$\begin{bmatrix} \mu & \lambda \\ \nu & K \end{bmatrix} = [F]$	Chain matrix of a digital 2-port
$\begin{bmatrix} A & B \\ C & D \end{bmatrix}$	Chain matrix of an analog 2-port network
$\lvert\tilde{F}\rvert$	Determinant of $[\tilde{F}]$

$\|F\|$	Determinant of [F]
Δ	Determinant of a square matrix
$Z_a(s)$	Impedance of a series element in a ladder network
Z_1	$Z_a(s)$ with s replaced by $(z-1)/(z+1)$
$Y_b(s)$	Admittance of a shunt element in a ladder network
Y_2	$Y_b(s)$ with s replaced by $(z-1)/(z+1)$
$\begin{bmatrix} \mu_1 & \lambda_1 \\ \nu_1 & K_1 \end{bmatrix} = [F_s]$	Chain matrix of a digital 2-port corresponding to the series element of an LC ladder
$\begin{bmatrix} \mu_2 & \lambda_2 \\ \nu_2 & K_2 \end{bmatrix} = [F_p]$	Chain matrix of a digital 2-port corresponding to the shunt element of an LC ladder
N^T	Digital 2-port whose transfer matrix is the transpose of the digital 2-port N
$[F_p]_T$	Chain matrix of the digital 2-port N^T
$[F_r]$	Chain matrix of the digital 2-port obtained by reversing the ports of a digital 2-port whose chain matrix is [F]
rms	Root-mean square
DFT	Discrete Fourier transform
FFT	Fast Fourier transform
2-D	Two-dimentional
IIR	Infinite-duration impulse response
FIR	Finite-duration impulse response

z_1, z_2	Complex variables
$\underline{X}$	Vector of design parameters

CHAPTER 1

INTRODUCTION

1.1 General:

Digital filters have come to play a greater role in recent times in signal processing. They serve the same purpose of spectrum shaping as the analog filters do. Though the analog methods and components have been the primary vehicle in many diverse fields that call for filtering applications, the digital techniques, of late, are entering the realm of analog counterparts. This has been made possible by the tremendous developments achieved in the fields of digital computers and semiconductor device technology.

The increasing use of digital filters, implemented by special purpose hardware, is due to their great potential and hence they are finding more and more applications. The guaranteed accuracy and essentially perfect reproducibility are two of the many significant advantages to be derived from them. In addition, the performance of digital systems is almost drift-free and for this reason digital filtering has become inimitable. To quote one instance, in area like the moving target indicating (MTI) radars analog filtering could be unreliable and hence digital filtering is preferable. The absence of impedance matching problem in digital filters makes the design simpler. For very low frequency applications, e.g., seismic data processing, analog components may be unwieldy, but since the size of digital components does not depend primarily on the frequency of interest, digital filter is the immediate

choice. Digital filters are highly flexible in the sense that the filter characteristics can be altered easily by chainging the contents of the coefficient registers. Another attractive feature of digital filters is their time-multiplexing capability. Different channels can time-share the same main arithmetic unit of a digital hardware. This has the potential of reducing the overall hardware cost. Though there are some disadvantages in the use of digital filters such as nonlinear effects, e.g., overflow oscillations, limit cycles, and problems of improper scaling, the many advantages listed above would make digital filtering an attractive alternative to analog filtering.

1.2 Historical Background:

The impact made by digital signal processing as evidenced in the foregoing section is so great that it is worth tracing its history. The field of digital signal processing emerged as a major engineering discipline only in the mid 1960's. The availability of high speed digital computers has been instrumental in the continuous growth of the many theoretical ideas constituting the main body of digital signal processing, while the overwhelming achievements made in semiconductor device technology, such as the large scale integration (LSI) techniques, have led to the implementation of digital filters and spectrum analysers by special purpose hardware for real-time applications. The two significiant contributions in digital signal processing are: i) the design of digital filters by the method of bilinear z-transform applied to analog counterparts [1], and ii) the development of a fast method of computing the discrete Fourier transform known as the fast Fourier transform (FFT) [2]. The significance of the FFT method lies in the reduction, by one to two

orders of magnitude for most practical problems, in computing time for the discrete Fourier transform (DFT).

Later, schemes were proposed for the implementation of digital filters and FFT processors by low priced digital components [3-12]. This gave the required impetus, in the 1970's, to the proposition of digital realizations having desirable properties like low coefficient sensitivity, roundoff error and hardware simplicity etc. [13-31]. However, these realizations have to be examined with respect to other properties like limit cycles, scaling requirements etc.

1.3 Digital Filter Realizations:

As pointed out in the previous sections the field of digital signal processing comprises essentially of two major areas, namely, digital filtering and spectrum analysis. Digital filtering deals with the finite-duration impulse response (FIR) and infinite-duration impulse response (IIR) filters. The spectrum analysis is concerned with the computation of discrete spectrum using FFT methods. In what follows the different realizations of digital filters will be discussed.

The two widely used synthesis of one and two-dimensional (2-D) FIR filters are i) windowing technique, and ii) frequency sampling technique [32-34]. The design of one-dimensional IIR filters is greatly aided by the known analog approximation methods through the use of the bilinear z transform. However, not many procedures are available for the design of 2-D IIR filters [35-37].

When digital filters are implemented by means of dedicated

hardware the coefficient and signal word lengths are both finite. As a result special care must be exercised with regard to stability and sensitivity in realizing a filter transfer function. Though FIR filters are unconditionally stable, problems of stability and sensitivity arise in realizing IIR filters. Naturally one must examine different possible structures. Conventionally there are three methods of realizing an IIR digital filter, namely, the direct, the cascade and the parallel methods [32-34]. In the direct method the digital transfer function is realized as a single input-output relation. In the cascade method the given transfer function is expressed as a product of first-order and or second-order functions and the individual function realized in the direct form and then cascaded. The parallel method requires the transfer function to be expressed in a partial fraction form, then each term realized in a direct form and then added. The sensitivity associated with the direct form is poor when compared to that associated with the other two forms. In [38], it is reported that for any reasonably complex filter with steep transitions between pass and stop bands the use of the direct form should be avoided. It is further suggested that from the point of view of roundoff noise the parallel form is better than the cascade one and that the direct form should be avoided at any rate.

Recently there has been great interest in proposing different digital realizations with a view that some of them might be most suitable from the point of view of hardware implementation [13-31,62]. In particular the works cited in [15] and [16] pertain to the class of cascade structures with second-order sections. In [14] a new class of structures known as lattice or ladder structures has been proposed,

which are especially useful in speech research. Another interesting type of structure proposed in [13,21-28] is known as the wave digital structure and has received much attention lately. Specifically, this method is based on imitating doubly terminated LC ladder structures. Instead of the voltages and currents, incident and reflected voltage or current waves are used as the input and output signals in the wave digital structures. Using bilinear z transform, each two-terminal element in the analog filter is transformed to a corresponding two-terminal wave digital element. However, direct interconnection of these wave digital elements in a ladder is forbidden, in general, due to the incompatibility of waves between the elements. So digital "adapters" are used to interconnect the different wave digital elements such that the waves are made compatible. The use of these adapters in these wave digital structures, however, seems to make the design procedure more complicated.

1.4 Frequency Transformations and BP and BS Filters:

All the realizations that were mentioned in the previous section deal basically with lowpass transfer functions. Such functions are realized from the appropriate analog functions in conjunction with the bilinear z transform. It has been shown in [39] that the corresponding frequency domain approximation problems for digital and analog filters are equivalent in the sense that one has a solution if and only if the other has a solution. Hence the well-known analog approximations in the frequency domain can be used to design digital filters. This implies that digital filters with highpass or bandpass or bandstop characteristics can be designed using the appropriate analog frequency transformations via the bilinear z transform. However, it is very laborious to design

such filters using the appropriate frequency transformations in the analog domain. To alleviate this problem, frequency transformations were first proposed [40] for digital filters by which a prototype lowpass digital filter can be transformed into another lowpass or highpass or bandpass or bandstop filter. There, a digital transformation of the form $z^{-1} \rightarrow g(z^{-1})$ is first assumed where $g(z^{-1})$ is an allpass function (of first-order for lowpass or lowpass and lowpass to highpass and second-order for lowpass to bandpass and bandstop) and then the coefficients of $g(z^{-1})$ in terms of the known specifications are determined.

Using these frequency transformations in the digital domain, bandpass and bandstop filters have been designed [4] from a prototype lowpass digital filter where only the center frequency could be varied. Design of lowpass to lowpass and lowpass to highpass filters by a direct replacement of z^{-1} by the appropriate $g(z^{-1})$ is not possible due to the presence of delay-free loops in the structure [4]. Very recently a Fettweis' wave digital structure for bandpass and bandstop filter with variable center frequency and bandwidth has been derived with no delay-free loop in the digital structure [41].

1.5 Two-dimensional Digital Filters:

The digital structures mentioned so far all aim at realizing one-dimensional transfer functions. As noted earlier two-dimensional (2-D) digital filters form an important class to be studied. The motivation for the study of 2-D digital filtering arises from its wide range of applications. For example, areas such as picture processing which includes weather photos, air reconnaissance pictures and medical

X-rays and areas where seismic records, magnetic data and electron micrographs are to be processed call for 2-D digital filtering.

Approximation and stability are the two major problems in the design of 2-D IIR filters, though these problems are virtually nonexistent in FIR filters. The design of a 2-D digital filter consists in choosing the coefficients of its 2-D transfer function so as to approximate a given spatial frequency response. Synthesis procedures for 2-D FIR filters are all readily extendable from the corresponding one-dimensional procedures [32]. However, very few procedures are avilable for the synthesis of 2-D IIR filters [35-37]. After the design, stability test must be performed. Though some stability tests have been proposed [35,42], they are difficult to carry out. If the designed filter is unstable then it must be stabilized using the available stabilization procedure [35]. However, this is also difficult to apply and hence the need for a procedure which automatically guarantees stability. When a 2-D IIR filter is designed from a corresponding 2-variable passive analog function via the double bilinear z transform, then the resulting digital filter is stable. To this end a method has been proposed in [43] to obtain a circularly symmetric 2-D IIR filter transfer function in conjunction with some optimization procedure.

So far very little effort is directed towards the realization of a 2-D IIR filter transfer function. A continued fraction approach [44] has been adopted to obtain different digital realizations for a 2-D IIR filter transfer function. However, the sensitivity and roundoff noise of these structures have not been determined.

1.6 Scope of the Thesis:

This Thesis proposes a new type of wave digital filter realization derived from a doubly terminated lossless network. It is shown that for a given analog network eight different digital realizations are possible, all being canonic with respect to both multipliers and delays. Further, a method is proposed for realizing bandpass and bandstop filters with variable center frequency and bandwidth using the proposed digital realizations. It is also shown how to derive the appropriate frequency transformations for digital filters in a simple manner from the analog counterparts. The floating-point coefficient sensitivity and roundoff noise of the proposed digital realizations are also studied. The procedure for the proposed one-dimensional wave digital realization is extended to the case of a 2-D digital filter realization.

Specifically the topics discussed are as follows:

In chapter 2, the frequency transformations for digital filters, derived earlier by Constantinides, are established in a very simple manner starting from the analog counterparts. In order to do so, it is first shown that a reactance transformation in the analog domain always corresponds to a stable allpass transformation in the digital domain and vice versa.

In chapter 3, a new type of wave digital filter structure is proposed. A doubly terminated, lossless network is first described by a wave or scattering matrix where the incident and reflected waves at the two ports are related to the voltages and currents at the respective

ports through the chain parameters of the network. Then, using bilinear z transform, the wave matrix of the analog network is transformed into a chain matrix description of a digital two-port, where the digital inputs and outputs are identified with the respective incident and reflected waves at the ports of the analog network. A realization is then obtained corresponding to this chain matrix of the digital two-port. Due to their low sensitivities to element variations, doubly terminated LC ladders are considered in deriving the wave digital structures. Both canonic and non-canonic digital two-port realizations corresponding to the different series and shunt elements of the ladder are obtained. For a given analog network eight different digital realizations are obtained, all being canonic with respect to both multipliers and delays.

Using the results of chapters 2 and 3, a design method is proposed in chapter 4 for realizing bandpass and bandstop digital filters. In these filters the center frequency and bandwidth can be varied independently by simply varying the multiplier values. A further advantage of this realization is that a reduction in the total number of coefficient registers is achieved.

The floating-point coefficient sensitivity and roundoff noise analyses of the proposed wave digital structures are detailed in chapter 5. For sensitivity analysis an rms value defined in [60] is used to measure the deviation of the actual frequency response from the ideal one when the multiplier coefficients are rounded for implementation. The rms value so defined is computed for second-order and seventh-order filters realized in the i) conventional form and ii) proposed wave digital form. It is found that the proposed wave digital realization has a

better sensitivity than the conventional form and is comparable to Fettweis' new structure [60]. The roundoff noise for a seventh-order filter is studied by simulating it on a digital computer. It is found that the proposed wave digital realizations have a higher signal to noise ratio than the conventional structure and is comparable to Fettweis' new structure [60].

Finally in chapter 6, the proposed one-dimensional wave digital realization procedure is extended to the case of a 2-D digital realization. An example of realizing a circularly symmetric 2-D wave digital filter is considered, where a procedure is outlined as to how to go about choosing a particular network structure and then obtain the element values using a known optimization procedure to approximate the desired spatial frequency response. Contour plots for the magnitude response are obtained for i) the wave digital realization and ii) the direct form realizing the same 2-D transfer function. The results show that the 2-D wave digital structure exhibits much lower sensitivity to multiplier coefficient rounding than the direct realization.

CHAPTER 2

FREQUENCY TRANSFORMATIONS FOR DIGITAL FILTERS

2.1 Introduction:

The frequency transformations in the analog domain are well known [53]. A prototype lowpass (LP) analog filter may be converted to a highpass (HP) or a bandpass (BP) or a bandstop (BS) filter using appropriate frequency transformations. These transformations preserve the basic characteristics of the amplitude response, such as ripple magnitude in the stopbands and passbands while changing other characteristics such as the cutoff frequencies or the number of stopbands and passbands.

Constantinides [40] first proposed a set of frequency transformations in the digital domain which play the same role as the frequency transformations in the analog domain. He first assumes a transformation of the form $z^{-1} \rightarrow g(z^{-1})$ where $g(z^{-1})$ is an allpass function, then determines the coefficients of $g(z^{-1})$ from the known specifications. With the appropriate $g(z^{-1})$, one can design another LP, or a HP or a BP or a BS digital filter from a prototype lowpass one by a mere substitution of z^{-1} by $g(z^{-1})$ in the prototype filter.

The purpose of this chapter is to show [45] that all the spectral transformations due to Constantinides are derivable in a simple,,

straightforward manner from the well known transformations in the analog domain in conjunction with the bilinear z transform. It is shown [45] further that a reactance transformation in the analog domain always corresponds to an allpass transformation in the digital domain and vice versa. These results are used later in Chapter 4 to obtain BP and BS filters with variable center frequency and bandwidth by varying the multiplier coefficients.

2.2 Derivation of the Frequency Transformations for Digital Filters:

It is well known that digital filters may be designed using the known approximation techniques for the analog filters through the bilinear transformation [32-34]

$$s = \frac{1-z^{-1}}{1+z^{-1}} \qquad (2.1)$$

In view of (2.1), it is also known that

$$\omega = \tan \Omega T/2 \qquad (2.2)$$

where ω = frequency variable for the analog filter;

Ω = frequency variable for the digital filter; and

T = sampling period.

Let $H(z^{-1})$ be the transfer function of a given prototype digital filter. Let the corresponding prototype analog filter obtained by using (2.1), that is

$$z^{-1} = \frac{1-s}{1+s} \tag{2.3}$$

be T(s). Then

$$T(s) = H\left(\frac{1-s}{1+s}\right) \tag{2.4}$$

Now, let us transform the prototype analog filter (2.4) into another filter through the reactance transformation

$$s \rightarrow f(s) \tag{2.5}$$

It is well known that such a transformation preserves some important basic characteristics of the amplitude response (such as ripple magnitude in the stop and pass bands) while changing other characteristics (such as the cutoff frequencies or the number of stop and pass bands).

The transfer function of the new analog filter is

$$T_1(s) = T\,[f(s)] = H\left[\frac{1-f(s)}{1+f(s)}\right] \tag{2.6}$$

Let the corresponding digital filter obtained by using (2.1) be

$$H_1(z^{-1}) = T_1(s)\Big|_{s=\frac{1-z^{-1}}{1+z^{-1}}} \tag{2.7}$$

Hence

$$H_1(z^{-1}) = H\left[\frac{1-f(s)}{1+f(s)}\right]_{s=\frac{1-z^{-1}}{1+z^{-1}}}$$

$$= H(g(z^{-1})), \text{ say} \qquad (2.8)$$

where

$$g(z^{-1}) = \frac{1 - f\left(\frac{1-z^{-1}}{1+z^{-1}}\right)}{1 + f\left(\frac{1-z^{-1}}{1+z^{-1}}\right)} \qquad (2.9)$$

Next we show that, when $f(s)$ is a reactance function, $g(z^{-1})$ is an allpass function. Let

$$f(s) = \frac{N(s)}{D(s)} \qquad (2.10)$$

where $N(s)$ and $D(s)$ may be either odd or even polynomial. So,

$$\frac{1-f(s)}{1+f(s)} = \frac{D(s)-N(s)}{D(s)+N(s)} \qquad (2.11)$$

Let $s=s_o$ be a zero of $D(s) + N(s)$. That is,

$$D(s_o) + N(s_o) = 0 \qquad (2.12)$$

Then for $s=-s_o$, the numerator of (2.11) is $D(-s_o) - N(-s_o)$. When $D(s)$ is even and $N(s)$ is odd, then

$$D(-s_o)-N(-s_o) = D(s_o)+N(s_o) = 0 \tag{2.13}$$

On the other hand, when $D(s)$ is odd and $N(s)$ is even, then

$$\begin{aligned} D(-s_o)-N(-s_o) &= -D(s_o)-N(s_o) \\ &= -D(s_o) + N(s_o)) \\ &= 0 \end{aligned} \tag{2.14}$$

Thus, in either case we see that if s_o is a pole of $\frac{1-f(s)}{1+f(s)}$, then $-s_o$ is a zero of the same function. Since $f(s)$ is a reactance function, the poles of $\frac{1-f(s)}{1+f(s)}$ lie on the l.h. plane and hence the poles of $g(z^{-1})$ lie on the interior of the circle $|z| < 1$ while the zeros of $g(z^{-1})$ lie on the exterior of the unit circle. Further, a pole of $g(z^{-1})$ at $z=z_o$ has a mirror image zero at $z=1/z_o$ and vice versa. Hence, $g(z^{-1})$ is an allpass function.

Thus, given a prototype digital filter $H(z^{-1})$, we may obtain another digital filter by using the spectral transformation,

$$z^{-1} \rightarrow g(z^{-1}) \tag{2.15}$$

where $g(z^{-1})$ is an allpass digital filter. This transformation again retains the basic amplitude characteristics while altering other characteristics such as the cutoff frequency, the number of pass and stop bands,

etc.

Using equation (2.9) we may now derive all the results given by Constantinides [40].

(a) LP-LP Transformation:

Consider first a prototype analog filter having a cutoff frequency of ω_c and let Ω_c be the cutoff frequency of the corresponding digital filter. Now let ω_β and Ω_β be the cutoff frequencies of the new lowpass analog filter and the corresponding digital filter. Then,

$$f(s) = \left(\frac{\omega_c}{\omega_\beta}\right) s \tag{2.16}$$

and from (2.9),

$$g(z^{-1}) = \frac{1-\left(\frac{\omega_c}{\omega_\beta}\right)\frac{1-z^{-1}}{1+z^{-1}}}{1+\left(\frac{\omega_c}{\omega_\beta}\right)\frac{1-z^{-1}}{1+z^{-1}}} \tag{2.17}$$

Eqn. (2.17) can be rearranged to give

$$g(z^{-1}) = \frac{z^{-1} - \alpha}{1 - \alpha z^{-1}} \tag{2.18}$$

where

$$\alpha = \frac{\omega_c - \omega_\beta}{\omega_c + \omega_\beta} = \frac{\sin(\frac{\Omega_c - \Omega_\beta}{2})T}{\sin(\frac{\Omega_c + \Omega_\beta}{2})T} \tag{2.19}$$

(b) LP-HP Transformation:

Next, consider a lowpass to highpass transformation. Let ω_c and ω_β be the critical frequencies of the prototype lowpass analog filter and the resulting highpass filter respectively. Let Ω_c and Ω_β be the corresponding ones for the digital lowpass and highpass filters. Then,

$$f(s) = \omega_c \omega_\beta \frac{1}{s} \tag{2.20}$$

and using (2.9), we get

$$g(z^{-1}) = \frac{1 - \omega_c \omega_\beta \frac{1+z^{-1}}{1-z^{-1}}}{1 + \omega_c \omega_\beta \frac{1+z^{-1}}{1-z^{-1}}} \tag{2.21}$$

Equation (2.21) can be rearranged to give

$$g(z^{-1}) = - \left(\frac{z^{-1}+\alpha}{1+\alpha z^{-1}}\right) \tag{2.22}$$

where

$$\alpha = -\frac{1-\omega_c\omega_\beta}{1+\omega_c\omega_\beta} = -\frac{\cos(\frac{\Omega_c+\Omega_\beta}{2})T}{\cos(\frac{\Omega_c-\Omega_\beta}{2})T} \qquad (2.23)$$

(c) LP-BP Transformation:

Now let us determine $g(z^{-1})$ for the bandpass case. Let ω_c and Ω_c be the cutoff frequencies of the prototype analog and corresponding digital lowpass filters. Let ω_o, ω_1 and ω_2 be the center frequency, the lower and upper cutoff frequencies of the analog bandpass filter. Let Ω_o, Ω_1 and Ω_2 be the corresponding ones for the digital bandpass filter. Then we known that the analog lowpass and bandpass transformation is [53]

$$f(s) = \omega_c \frac{s^2+\omega_o^2}{Bs} \qquad (2.24)$$

where

$$B = \omega_2-\omega_1 \qquad (2.25a)$$

and

$$\omega_o^2 = \omega_1\omega_2 \qquad (2.25b)$$

Hence from (2.9), the transformation needed to convert a digital lowpass to a digital bandpass filter is

$$g(z^{-1}) = \frac{1-\frac{\omega_c}{B}\frac{\{(1-z^{-1})^2+\omega_o^2(1+z^{-1})\}^2}{1-z^2}}{1+\frac{\omega_c}{B}\{\frac{(1-z^{-1})^2+\omega_o^2(1+z^{-1})^2}{1-z^2}\}} \qquad (2.26)$$

or

$$g(z^{-1}) = -\frac{z^{-1} - \frac{2\alpha K}{K+1}z^{-1} + \frac{K-1}{K+1}}{\frac{K-1}{K+1}z^{-2} - \frac{2\alpha K}{K+1}z^{-1} + 1} \qquad (2.27)$$

where

$$\alpha = \frac{1-\omega_o^2}{1+\omega_o^2} = \cos(\Omega_o T) \qquad (2.28)$$

and

$$K = \frac{\omega_c}{B}(1+\omega_o^2) = \tan(\frac{\Omega_c T}{2})\cot(\frac{\Omega_2-\Omega_1}{2})T \qquad (2.29)$$

Equations (2.27), (2.28) and (2.29) are identical to those given in [40].

(d) LP-BS Transformation:

Finally, we consider the lowpass to band-elimination transformation. Let ω_c and Ω_c be the cutoff frequencies of the lowpass analog filter and its corresponding lowpass digital filter. Let ω_o, ω_1 and ω_2 be the center frequency, the lower and upper cutoff frequencies of the analog bandstop filter, and let Ω_o, Ω_1 and Ω_2 be the corresponding ones of

the bandstop digital filter. Then, the required lowpass to bandstop transformation is [53]

$$f(s) = \omega_c B \frac{s}{s^2+\omega_o^2} \tag{2.30}$$

Therefore, from (2.9),

$$g(z^{-1}) = \frac{1 - \dfrac{\omega_c B(1-z^{-2})}{(1-z^{-1})+\omega_o^2(1+z^{-1})^2}}{1 + \dfrac{\omega_c B(1-z^{-2})}{(1-z^{-1})^2+\omega_o^2(1+z^{-1})^2}} \tag{2.31}$$

Simplifying (2.31), we get finally

$$g(z^{-1}) = \frac{z^{-2} - \dfrac{2\alpha}{1+K} z^{-1} + \dfrac{1-K}{1+K}}{\left(\dfrac{1-K}{1+K}\right) z^{-2} - \dfrac{2\alpha}{1+K} z^{-1} + 1} \tag{2.32}$$

where

$$\alpha = \frac{1-\omega_o^2}{1+\omega_o^2} = \cos(\Omega_o T) \tag{2.33}$$

and

$$K = \frac{\omega_c B}{1+\omega_o^2} = \tan\left(\frac{\Omega_c T}{2}\right) \tan\left(\frac{\Omega_2-\Omega_1}{2}\right) T \tag{2.34}$$

2.3 Conclusions:

Thus summarizing, corresponding to any transformation $s \to f(s)$ for an analog filter, the corresponding transformation for the digital filter is $z^{-1} \to g(z^{-1})$ where $g(z^{-1})$ is given by (2.9); if $f(s)$ is a reactance function, then $g(z^{-1})$ is an allpass function and vice versa. In the latter case, $f(s)$ may be shown to be

$$f(s) = \left[\frac{1-g(z^{-1})}{1+g(z^{-1})}\right]_{z^{-1} = \frac{1-s}{1+s}} \tag{2.35}$$

CHAPTER 3

A NEW TYPE OF WAVE DIGITAL FILTER

3.1 Introduction:

There has been a great deal of effort directed towards the realization of digital filters having low sensitivities to multiplier variations.[13-31] Fettweis[13,21-28] proposed a class of digital filters known as the wave digital filters which exhibit much less variations in the transfer characteristics than the conventional form of digital filters do. Using Fettweis' technique, Renner and Gupta[18,19] have given procedures for designing digital filters patterned after maximum available power (MAP) networks.

Fettweis' method is based on imitating the doubly terminated LC-ladder structures. Instead of the voltages and currents, incident and reflected voltage or current waves are used as the input and output signals in wave digital filters. Using the bilinear z transformation, each two-terminal element in the analog filter is transformed into a corresponding two-terminal (one-port) digital element, with the incident and reflected waves as digital input and output.

When different digital elements are to be interconnected to form a ladder, the port resistances of the different digital elements must be altered in order that the incident and reflected waves at different ports, which in turn implies the different port voltages and currents, be compatible. In order to achieve this, Fettweis uses "digital adapters"

at the appropriate places so as to make the waves at different ports compatible. However, for physical realizability condition, the resulting digital structure must have no delay-free loops. In Fettweis' method, when the port resistances are arbitrary, then delay-free loops appear when different ports are interconnected.[13] To avoid this, extra delays (called the unit elements) have to be inserted between the ports of the adapters. This results in structures which are noncanonic in delays and multipliers. Later, by constraining the port resistances to have a definite relation, Fettweis showed that the structure obtained thus will be free of delay-free loops and hence physically realizable while it is canonic in both multipliers and delays [21].

We propose here an alternate method of realizing a wave digital filter starting with a doubly terminated lossless analog two-port network [46]. The lossless network is first described by a wave or scattering transfer matrix in which the incident and reflected waves at the two ports are related to the voltages and currents at the respective ports through the ABCD matrix of the two-port. Then using the bilinear z transform the wave matrix of the analog network is transformed into a chain matrix description of a digital two-port where the digital inputs and outputs are identified with the respective incident and reflected waves at the ports of the analog network. A realization is then obtained corresponding to this chain matrix of the digital two-port.

When the lossless analog two-port is a cascade of two-ports, then the overall wave matrix is the product of the wave matrices of the individual two-ports. Hence, the overall chain matrix of the corresponding

digital two-port is the product of the chain matrices corresponding to the individual two-ports. The submatrices may be realized and cascaded without the need for any 'adapters' to obtain the overall digital realization. In order that the resulting structure be physically realizable, i.e., the present output sample be computed from the present and past input samples and past output samples, there should be no delay-free loop in the digital structure. It is possible that a delay-free loop may exist when digital two-ports are cascaded even though there may be no delay-free loop in the individual two-ports. However, if we ensure that there is no delay-free path between the input and the output of port 1, say, then no delay-free loop will be present in the overall structure. Basing this fact, in section 3.5 conditions on the port resistances are derived such that the resulting digital realization will have no delay-free loops. The resulting structure will also be canonic in both delays and multipliers.

3.2 Characterization of the Wave Digital Two-port:

Consider Fig. 3.1, where the black box $\tilde{N}$ may contain an interconnection of linear elements. Now define the wave variables $(\tilde{a}_i, \tilde{b}_i)$, i=1,2 by

$$\begin{bmatrix} \tilde{a}_i \\ \tilde{b}_i \end{bmatrix} = \begin{bmatrix} 1 & R_i \\ 1 & -R_i \end{bmatrix} \begin{bmatrix} V_i \\ I_i \end{bmatrix}, \qquad (3.1)$$

where $\tilde{a}_i$ and $\tilde{b}_i$ are the incident and reflected waves, R_1 and R_2

are arbitrary port normalization constants at ports 1 and 2. The voltages and currents at the ports 1 and 2 of $\tilde{N}$ are further related by the ABCD matrix by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3.2}$$

Using (3.1) and (3.2) we may now express $(\tilde{a}_1, \tilde{b}_1)$ in terms of $(\tilde{b}_2, \tilde{a}_2)$ as

$$\begin{bmatrix} \tilde{a}_1 \\ \tilde{b}_1 \end{bmatrix} = \begin{bmatrix} \tilde{\mu} & \tilde{\lambda} \\ \tilde{\nu} & \tilde{k} \end{bmatrix} \begin{bmatrix} \tilde{b}_2 \\ \tilde{a}_2 \end{bmatrix} = [\tilde{F}] \begin{bmatrix} \tilde{b}_2 \\ \tilde{a}_2 \end{bmatrix} \tag{3.3}$$

where

$$\begin{aligned} \tilde{\mu} &= \frac{A+R_1C}{2} + \frac{B+R_1D}{2R_2} \\ \tilde{\lambda} &= \frac{A+R_1C}{2} - \frac{B+R_1D}{2R_2} \\ \tilde{\nu} &= \frac{A-R_1C}{2} + \frac{B-R_1D}{2R_2} \\ \tilde{k} &= \frac{A-R_1C}{2} - \frac{B-R_1D}{2R_2} \end{aligned} \tag{3.4}$$

It may be observed that the determinant of $[\tilde{F}]$ is

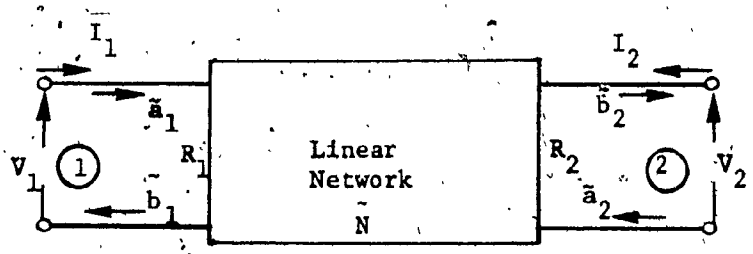


FIG.3.1 - An Analog 2-port containing an Interconnection of linear Elements.

$$|\tilde{F}| = \frac{R_1}{R_2}\,(AD-BC) \tag{3.5}$$

In general, the elements of $[\tilde{F}]$ are functions of s. If we now use the bilinear transformation [32-34]

$$s = \frac{z-1}{z+1} \tag{3.6}$$

and identify $\tilde{a}_1$ and $\tilde{a}_2$ with the input, and $\tilde{b}_1$ and $\tilde{b}_2$ with the output variables of a digital 2-port [52], then we may recognize (3.3) as the chain matrix description of a digital two-port. We shall write (3.3) with (3.6) substituted as

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} \mu & \lambda \\ \nu & k \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} = [F] \begin{bmatrix} b_2 \\ a_2 \end{bmatrix}, \tag{3.7a}$$

where

$$[F] = [\tilde{F}] \quad \text{with } s = \frac{z-1}{z+1}. \tag{3.7b}$$

If N is reciprocal, it is seen from (3.5) and (3.7b) that

$$|F| = \frac{R_1}{R_2} \tag{3.8}$$

Thus, given any two-port network N with port resistances

R_1 and R_2, we may describe a corresponding wave digital two-port N, whose chain matrix is given by (3.7). It is clear that if $\tilde{N}$ is a cascade of two-ports, say, $\tilde{N}_1, \tilde{N}_2, \ldots, \tilde{N}_m$, then the corresponding digital two-port is the cascade of the digital two-ports $N_1, N_2, \ldots N_m$ where N_i is the digital two-port corresponding to $\tilde{N}_i$; of course, it is assumed here that the output port resistance of $\tilde{N}_i$ is the same as the input port resistance of $\tilde{N}_{i+1}$.

3.3 Realization of the Digital Two-port:

We shall now consider the realization of a digital two-port starting with a doubly terminated analog network $\tilde{N}$ (Fig. 3.2). It is seen from Fig. 3.2 that

$$V_1 = V_s - I_1 R_s \tag{3.9}$$

$$V_2 = -I_2 R_L \tag{3.10}$$

Hence, from (3.1) and (3.10), we have

$$\tilde{a}_2 = \tilde{b}_2 \phi \tag{3.11}$$

and

$$\tilde{b}_2 = \frac{2V_2}{1+\phi} , \tag{3.12}$$

where

$$\phi = \frac{R_L - R_2}{R_L + R_2} \tag{3.13}$$

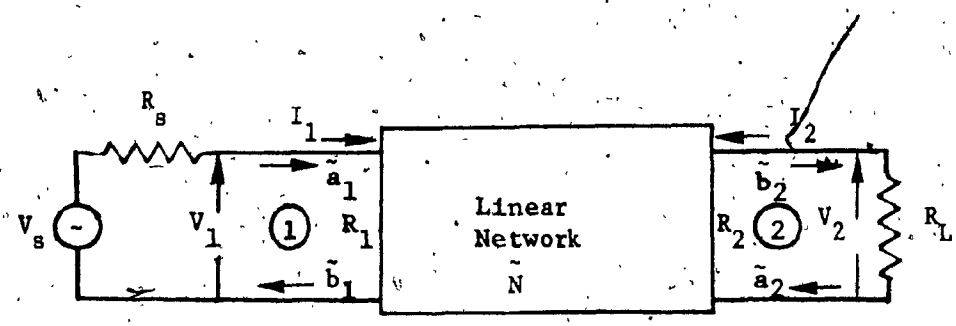


FIG. 3.2 - A doubly terminated analog network.

Also, from (3.1) and (3.9), we have

$$\tilde{a}_1+\theta\tilde{b}_1 = (1+\theta)\,\tilde{a}_s \tag{3.14}$$

where

$$v_s = \tilde{a}_s \,, \tag{3.15}$$

$$\theta = \frac{R_1-R_s}{R_1+R_s} \tag{3.16}$$

Hence,

$$\frac{\tilde{b}_2}{\tilde{a}_s} = \frac{2v_2}{(1+\phi)v_s} = \frac{2}{1+\phi}\,\frac{v_2}{v_s} \tag{3.17}$$

Also from (3.3) and (3.14),

$$(\tilde{\mu}+\tilde{\lambda}\phi)\tilde{b}_2 = (1+\theta)\tilde{a}_s-\theta(\tilde{\nu}+\phi\tilde{k})b_2$$

or

$$\frac{\tilde{b}_2}{\tilde{a}_s} = \frac{1+\theta}{\tilde{\mu}+\tilde{\lambda}\phi + \tilde{\nu}\theta + \tilde{k}\theta\phi} \tag{3.18}$$

If we denote

$$H(z) = \frac{v_2}{v_s} \quad \text{with} \quad s = \frac{z-1}{z+1} \tag{3.19}$$

then

$$\frac{b_2}{a_s} = \frac{2}{1+\phi}\, H(z)\,, \tag{3.20a}$$

where

$$\frac{b_2}{a_s} = \frac{1+\theta}{\mu+\lambda\phi+\nu\theta+k\theta\phi}\,, \tag{3.20b}$$

$$a_2 = b_2\phi\,, \tag{3.20c}$$

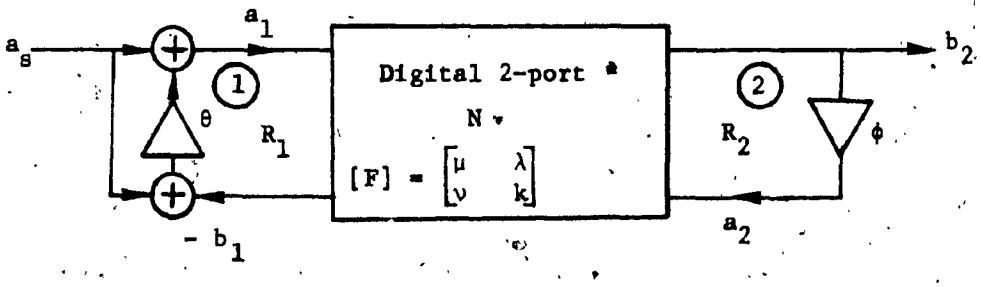
$$a_1 = (1+\theta)a_s - \theta b_1 \tag{3.20d}$$

The corresponding realization is shown in Fig. 3.3, where N is the digital two-port corresponding to $\tilde{N}$.

Thus given the realization $T(s) = \frac{V_2}{V_s}$ as a doubly terminated two-port $\tilde{N}$, we can obtain the corresponding realization for $H(z) = \frac{V_2}{V_s}$ with $s = \frac{z-1}{z+1}$ by using Fig. 3.3, where the digital two-port N is obtained from the corresponding analog network $\tilde{N}$.

Thus given the realization $T(s) = \frac{V_2}{V_s}$ as a doubly terminated two-port $\tilde{N}$, we can obtain the corresponding realization for $H(z) = \frac{V_2}{V_s}$ with $s = \frac{z-1}{z+1}$ by using Fig. 3.3, where the digital two-port N is obtained from the corresponding analog network $\tilde{N}$.

Until now we have not made any assumptions about $\tilde{N}$. However, we shall assume $\tilde{N}$ to be a lossless ladder since it is known [49] to have very low sensitivity with respect to element variations. Then the



$$\sigma = \frac{R_1 - R_s}{R_1 + R_s}$$

$$\phi = \frac{R_L - R_2}{R_L + R_2} \quad \because \; a_s = v_s$$

$$\frac{b_2}{a_s} = \frac{2}{1+\phi} H(z), \; H(z) = \left.\frac{V_2}{V_s}\right|_{s=\frac{z-1}{z+1}}$$

FIG. 3.3 The digital 2-port realization corresponding to the network in Fig. 3.2.

series elements can only be an L, C or an LC-parallel circuit*, while the shunt elements can only be an L, C or a series LC-circuit*. Thus, it is necessary to derive the digital two-ports corresponding to only these elements, which we shall do in succeeding sections. Then, we may cascade them to form N and use Fig. 3.3 to realize $H(z)$.

3.4 Design of Digital Two-ports Corresponding to the Case $R_1=R_2$ for all the Series and Shunt Elements in $\tilde{N}$:

Let a series element in $\tilde{N}$ be denoted by $Z_a(s)$, while a shunt element by $Y_b(s)$. Let Z_1 and Y_2 represent the functions with $s=(z-1)/(z+1)$. Then for a series element Z_a, the digital two-port description is

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} \mu_1 & \lambda_1 \\ \nu_1 & k_1 \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} = [F_s] \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \qquad (3.21)$$

with

$$\mu_1 = \frac{Z_1 + (R_1+R_2)}{2R_2} ,$$

---

*Any reactance function can always be realized in Foster's I or II form.

$$\nu_1 = -\frac{Z_1 + (R_2-R_1)}{2R_2} \quad ,$$

$$\lambda_1 = (1-\mu_1), \; k_1 = (1-\nu_1) \quad , \tag{3.22}$$

while for a shunt element y_b

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} \mu_2 & \lambda_2 \\ \nu_2 & k_2 \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} = [F_p] \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \quad , \tag{3.23}$$

where

$$\mu_2 = \frac{Y_2 + (G_1+G_2)}{2G_1}$$

$$\lambda_2 = \frac{Y_2 + (G_1-G_2)}{2G_1} \tag{3.24}$$

$$\nu_2 = (1-\mu_2), \; k_2 = (1-\lambda_2)$$

In the simple case when $R_1=R_2=R$ (say), (3.21) and (3.23) may be rearranged as

$$b_1 = a_2 + \frac{(\frac{1-\sigma}{2})(1-z^{-1})}{1+\sigma z^{-1}} (a_1-a_2)$$

$$b_2 = a_1 - \frac{(\frac{1-\sigma}{2})(1-z^{-1})}{1+\sigma z^{-1}} (a_1-a_2) \tag{3.25}$$

where $\sigma = (2R-L)/(2R+L)$

for the series element, and

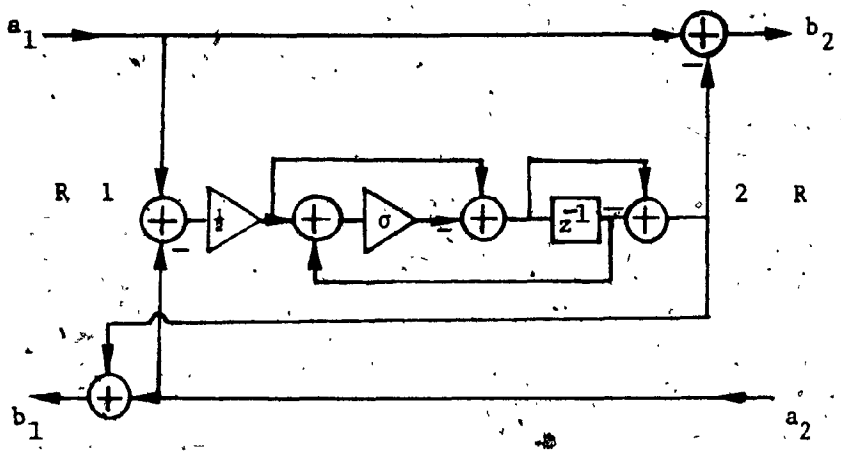
$$b_1 = a_2 - \frac{(\frac{1-\sigma}{2})\ (1-z^{-1})}{1+\sigma z^{-1}}\ (a_1+a_2)$$

$$b_2 = a_1 - \frac{(\frac{1-\sigma}{2})\ (1-z^{-1})}{1+\sigma z^{-1}}\ (a_1+a_2) \qquad (3.26)$$

where $\sigma = (2G-C)/(2G+C)$

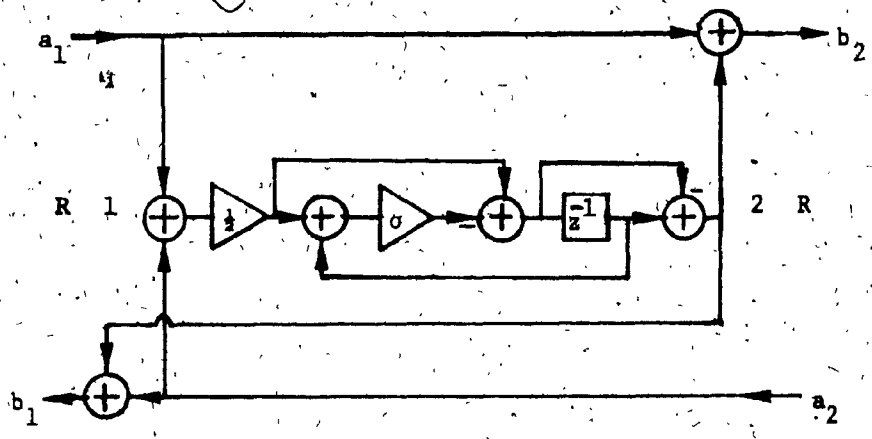
for the shunt element. For illustration, the corresponding realizations are shown for series L and shunt C in Fig. 3.4(a) and (b). Realizations for series C and shunt L may be obtained by changing z^{-1} to $-z^{-1}$ and L to 1/C in Fig. 3.4(a) and (b) respectively. Similarly, realizations may also be obtained for a parallel LC in the series arm and a series LC in the shunt arm. It should be pointed out that there are no delay-free loops in any of these realizations. However, when these are cascaded, delay-free loops appear, a situation which is similar to the one encountered in wave digital filters discussed in Refs. [13,18,19]. In order to overcome this difficulty, we introduce an extra delay element either in the forward path or in the return path where two sections are cascaded. It should be pointed out further that one should always choose either $R=R_L$ or $R=R_s$ in Fig. 3.2, so that in Fig. 3.3 either $\phi=o$ or $\theta=o$ in order to avoid a delay-free loop in the overall structure. However, this results in no loss of generality.

To illustrate the procedure a design example is considered. This is taken from [18]. Let it be required to design a third-order lowpass Butterworth filter with a cutoff frequency of 100 Hz and



$$\sigma = (2R-L)/(2R+L)$$

FIG. 3.4a - A digital realization for the series inductor where $R_1=R_2=R$.



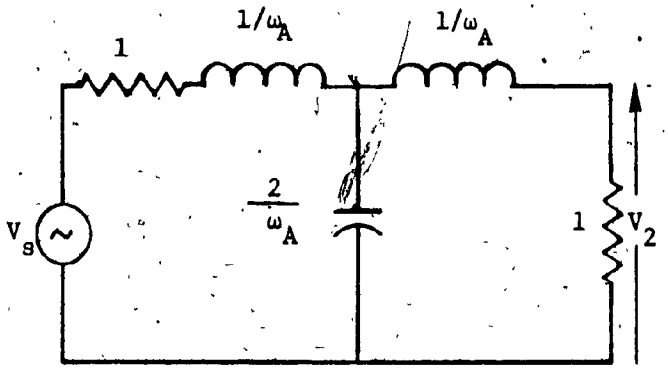
$$\sigma = (2G-C)/(2G+C)$$

FIG. 3.4b - A digital realization for the shunt capacitor where $R_1=R_2=R$.

sampling frequency of 10 KHz. Since the bilinear z transformation is being used, the cirtical frequency must be prewarped using [32-34]

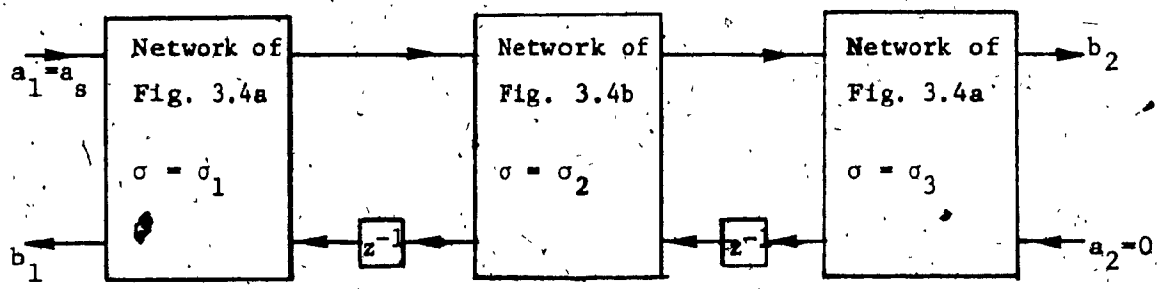
$$\omega_A = \tan\left(\frac{\omega_D T}{2}\right) \qquad (3.27)$$

where ω_A and ω_D correspond to the critical frequencies of the analog and digital filters respectively. The analog filter is shown in Fig. 3.5, with its corresponding digital structure in Fig. 3.6. In order to examine the effect of quantization of the multiplier coefficients, plots of the magnitude response of the wave digital filter of the above example are shown in Fig. 3.7 for different levels of fixed-point quantization. To make a valid comparison the same digital transfer function is realized in the conventional cascade form as shown in Fig. 3.8, and its corresponding plots are shown in Fig. 3.9. From the two plots, we observe that the shift in the magnitude response due to coefficient changes is less for the proposed wave digital realization than for the conventional cascade form. It is found that for this example, realization is possible even with word lengths of 5 bits for multipliers by the proposed method while a minimum of 15 bits are required for the conventional cascade form and 10 bits for the Fettweis' structure. The different parameters of interest are listed in Table 3.1. From the entries in the table, we observe that the proposed wave digital filter realization is more desirable than the conventional cascade form and comparable to the Fettweis' realization.



$$T(s) = \frac{V_2}{V_s} , \quad \omega_A = 0.031626266$$

FIG. 3.5 – A doubly terminated 3rd-order LP Butterworth filter of the example in Section 3.4.



$$\sigma_1 = -0.88172593 ,$$

$$\sigma_2 = -0.939062506 ,$$

$$\sigma_3 = \sigma_1$$

FIG. 3.6 – A noncanonic wave digital realization corresponding to the analog network of Fig. 3.5.

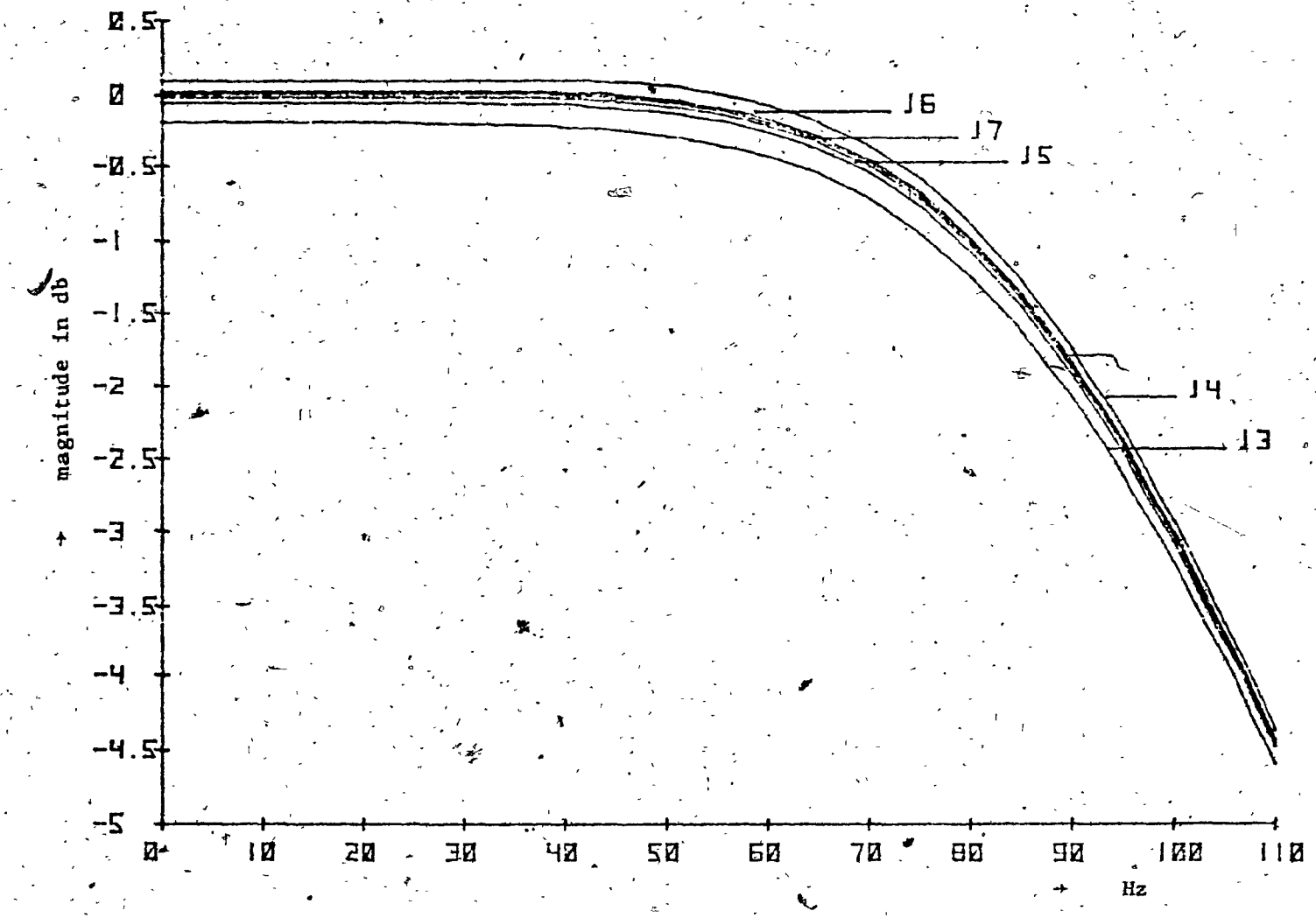
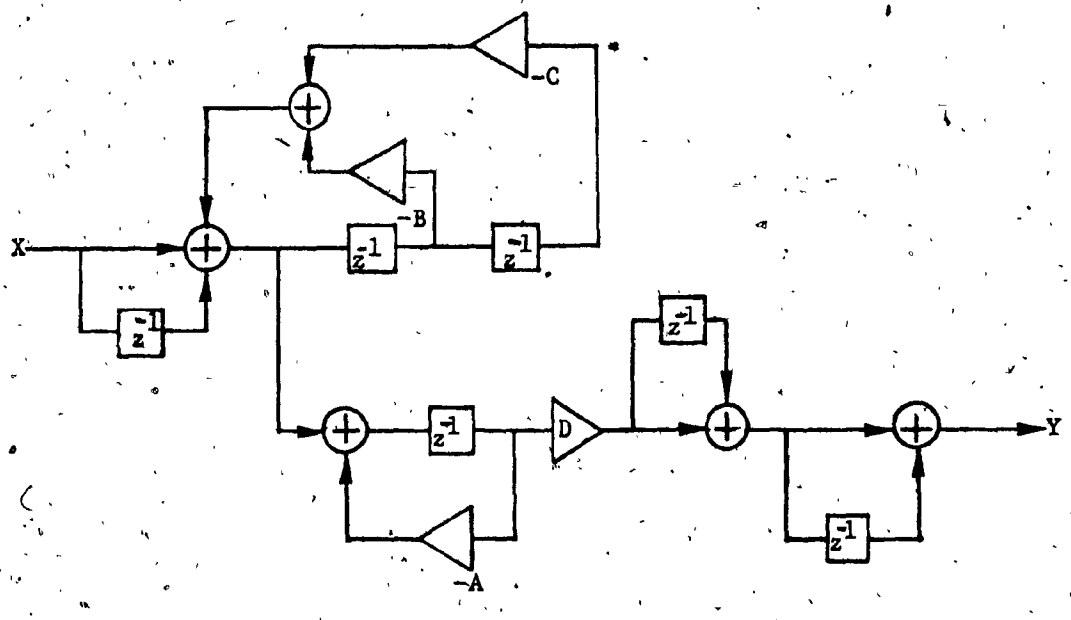


FIG. 3.7 - Magnitude response of the digital filter of Fig. 3.6 for different fixed-point quantizations of its multiplier coefficients.



$$\frac{Y}{X} = \frac{D(1+z^{-1})^3}{(1+Az^{-1})(1+Bz^{-1}+Cz^{-2})}$$

FIG. 3.8 - The conventional cascade realization of a 3rd-order LP Butterworth transfer function of the example in Section 3.4.

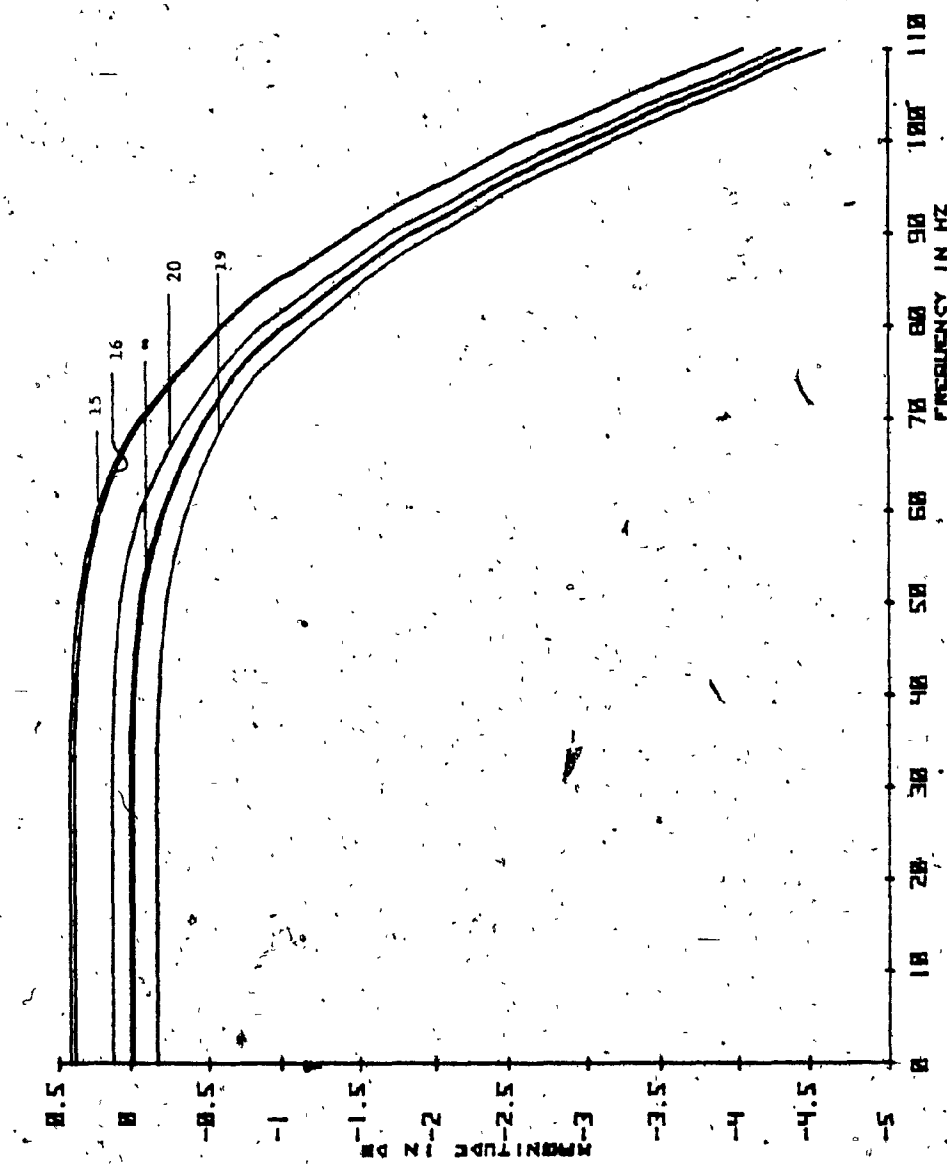


FIG. 3.9 - Magnitude response of the digital filter of Fig. 3.8 for different fixed-point quantization of its multiplier coefficients.

TABLE 3.1

Pertinent Features of the Digital Structures

CASCADE REALIZATION

Bits	15	16	17	18	19	∞
3 db freq. (Hz)	89.5	100	99.8	99.9	100	100
% error	-10.5	0	- 0.2	- 0.1	0	0
Gain at dc (db)	0.425	0.391	0.409	0.4	-0.16	0

FETTWEIS REALIZATION

Bits	15	16	17	18	19	∞
3 db freq. (Hz)	99.8	100.2	99.9	100	100	100
% error	- 0.2	0.2	- 0.1	0	0	0
Gain at dc (db)	- 0.0668	-0.0053	- 0.0293	0.005	0.005	0

PROPOSED FILTER

Bits	15	16	17	18	19	∞
3 db freq. (Hz)	99.9	100	100	100	100	100
% error	- 0.1	0	0	0	0	0
Gain at dc (db)	- 0.052	0.0151	-0.0174	-0.00118	-0.000917	0

$$\% \text{ error} = \frac{f - f_\infty}{f_\infty} \times 100$$

3.5 Canonic Realization of Wave Digital Two-ports:

Unitl now it had been assumed that the port resistances R_1 and R_2 were equal for each of the individual two-ports in N. Under this condition, even though the corresponding digital two-ports had no dealy-free loops, cascade of such two-ports had delay-free loops. In order to remove these delay-free loops, we had to introduce extra delays. We shall now show that by relaxing the condition $R_1=R_2$, we can obtain digital filters which are canonic with respect to both delays and multipliers [46].

The digital two-port descriptions corresponding to series and shunt elements are respectively given by (3.21) and (3.23) and may be rewritten [46] as

$$\begin{aligned} b_1 &= a_2 + \left(\frac{\nu_1}{\mu_1}\right)(a_1-a_2) \\ b_2 &= a_2 + \left(\frac{1}{\mu_1}\right)(a_1-a_2) \end{aligned} \qquad (3.28)$$

for the series element, and

$$\begin{aligned} b_1 &= a_2 + \left(\frac{\nu_2}{\mu_2}\right)(a_1+\sigma_2 a_2) \\ b_2 &= -a_2 + \left(\frac{1}{\mu_2}\right)(a_1+\sigma a_2) \\ \sigma &= R_1/R_2 \end{aligned} \qquad (3.29)$$

for the shunt element. These may be realized as shown in Fig. 3.10(a) and (b). It is seen from these figures that there are delay-free paths from a_2 to b_2 in the realization of both the series and shunt elements. Thus, if (ν_1/μ_1) and $(\frac{\nu_2}{\mu_2})$ are made to have no delay-free paths, then there will be no delay-free paths from a_1 to b_1; as a consequence, there will be no delay-free loops when two sections are cascaded. In order to ensure this, we should make sure that the numerators of $(\frac{\nu_1}{\mu_1})$ and $(\frac{\nu_2}{\mu_2})$ should be of at least one degree lower in z than their corresponding denominators.

We shall first show how we can achieve this for a series L. For this element, we may write

$$\frac{\nu_1}{\mu_1} = \frac{z(R_2-R_1+L) + (R_2-R_1-L)}{z(R_2+R_1+L) + (R_2+R_1-L)} \tag{3.30}$$

To ensure $(\frac{\nu_1}{\mu_1})$ to have no delay-free paths, we set

$$R_2-R_1+L = 0 \quad \text{or} \quad R_1=R_2+L \tag{3.31}$$

In this case the digital two-port description becomes

$$\begin{aligned} b_1 &= a_2 + \frac{(\sigma-1)z^{-1}}{1+\sigma z^{-1}} (a_1-a_2) , \\ b_2 &= a_2 + \frac{\sigma(1+z^{-1})}{1+\sigma z^{-1}} (a_1-a_2) , \end{aligned} \tag{3.32}$$

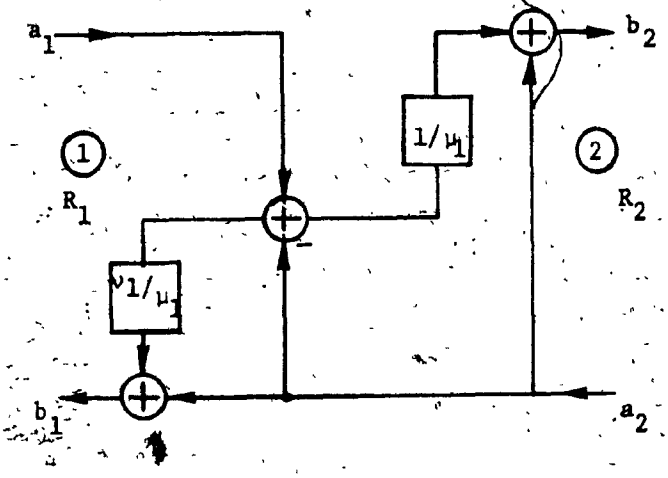
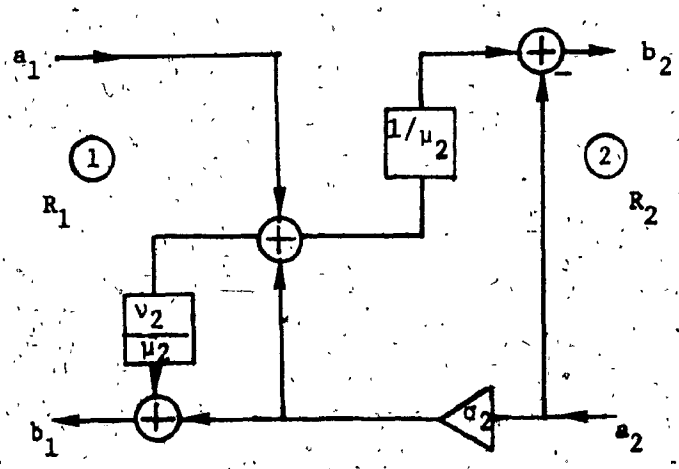


FIG. 3.10a - The digital 2-port realization of equation (3.28).



$$\sigma_2 = G_2/G_1 = R_1/R_2$$

FIG. 3.10b - The digital 2-port realization of equation (3.29).

where

$$\sigma = \frac{R_2}{R_1} = \frac{R_2}{(R_2+L)} \qquad (3.33)$$

A realization for (3.32) is shown in Table 3.2.

For a shunt capacitor, we have from (3.24)

$$\frac{\nu_2}{\mu_2} = \frac{(G_1-G_2-C)z + (G_1-G_2+C)}{(G_1+G_2+C)z + (G_1+G_2-C)} \qquad (3.34)$$

In order that $\frac{\nu_2}{\mu_2}$ have no delay-free path, we must set

$$G_1-G_2-C = 0$$

or (3.35)

$$G_1 = G_2+C$$

Then the digital two-port description becomes

$$b_1 = a_2\sigma + \frac{(1-\sigma)z^{-1}}{1+\sigma z^{-1}}(a_1+a_2\sigma)$$

$$b_2 = -a_2 + \frac{1+z^{-1}}{1+\sigma z^{-1}}(a_1+a_2\sigma) \qquad (3.36)$$

where

$$\sigma = G_2/G_1 \qquad (3.37)$$

A realization for (3.36) is shown in Table 3.2.

Next we shall obtain a realization for the parallel LC circuit in the series arm of a ladder. This may be done in a simple manner as follows: The impedance of the parallel LC circuit is

$$Z_a = \frac{1/c\ s}{s^2+1/LC} \tag{3.38}$$

With s replaced in (3.38) by $(1-z^{-1})/(1+z^{-1})$, equation (3.38) becomes

$$Z_1 = Z_a \Big|_{s=(1-z^{-1})/(1+z^{-1})}$$

$$= \frac{1/c\ (1-z^{-2})}{(1-z^{-1})^2 + \frac{1}{LC}(1+z^{-1})^2} \tag{3.39}$$

Equation (3.39) may be rearranged to give

$$Z_1 = (L/(1+LC)\ \frac{1-z^{-1}(\alpha+z^{-1})/(1+\alpha z^{-1})}{1+z^{-1}\ (\alpha+z^{-1})/(1+\alpha z^{-1})} \tag{3.40}$$

where

$$\alpha = (1-LC)/(1+LC) \tag{3.41}$$

Comparing Z_1 in (3.40) with that corresponding to a series inductor, we get the following: L for the series inductance is replaced by $L/(1+LC)$ for the parallel LC and z^{-1} for the series L is replaced by $g(z^{-1})$ for the parallel LC, where

$$g(z^{-1}) = z^{-1}\,(\alpha+z^{-1})/(1+\alpha z^{-1}) \tag{3.42}$$

The port normalization constants for the parallel LC case are related by

$$R_1 = R_2+L/(1+LC) \tag{3.43}$$

Thus, a realization for the parallel LC circuit in the series arm may be obtained from that corresponding to a series L by simply replacing z^{-1} by $g(z^{-1})$ where $g(z^{-1})$ is given by (3.42). The realization is shown in Table 3.2 with the multiplier values.

Next, we shall consider the realizations for the shunt elements. Let $[F_p]$ be the chain matrix of a digital two-port N_p corresponding to a shunt element of a ladder, and given by (3.23). Let N_p^T represent a digital two-port, whose transfer matrix is the transpose of that of N_p; such a two-port can be obtained from N_p by simply reversing the arrows in N_p.[50,51] Then the chain matrix of N_p^T is given by

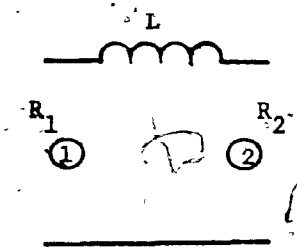
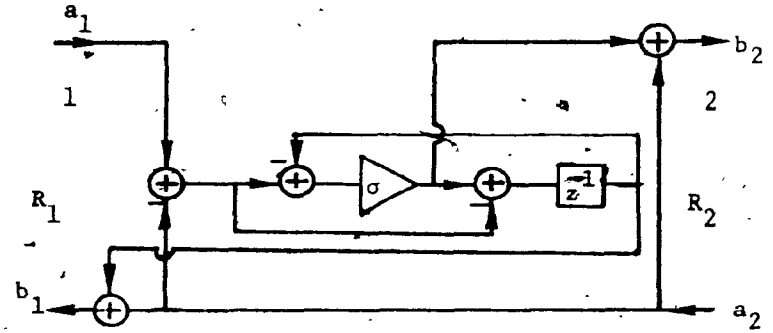
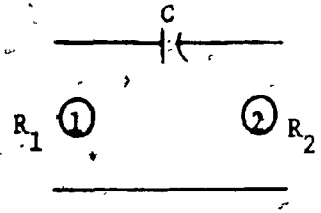
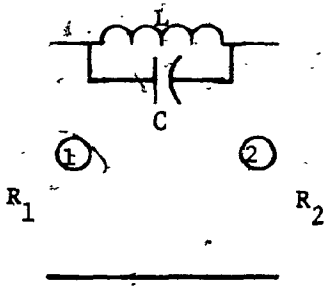
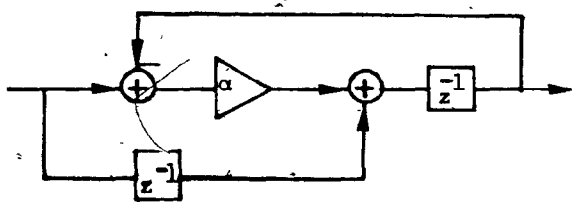
$$[F_p]_T = \frac{1}{\Delta}\begin{bmatrix}\mu_2 & \lambda_2\\ \nu_2 & k_2\end{bmatrix} \tag{3.44a}$$

where

$$\Delta = |F_p| = \frac{R_1}{R_2} \tag{3.44b}$$

TABLE 3.2

First Set of Realizations Corresponding to the Series Element Z_1 with **no Delay**-free Path from a_1 to b_1

Element	Corresponding Wave Digital Two-port	Relations
	 Network N_1	$\sigma = R_2/R_1$ $R_1 = R_2+L$
	Same as Network N_1 with z^{-1} replaced by $-z^{-1}$ Network N_2	$\sigma = R_2/R_1$ $R_1 = R_2+1/C$
	Same as Network N_1 with z^{-1} replaced by $g(z^{-1})$ in (3.19); a realization for $g(z^{-1})$ is shown here:  Network N_3	$\sigma = R_2/R_1$ $\alpha = \frac{1-LC}{1+LC}$ $R_1 = R_2+\frac{L}{1+LC}$

If we now identify Y_b with Z_a, G_1 with R_1 and G_2 with R_2, we see that (3.44) reduces to

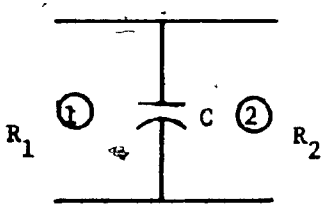
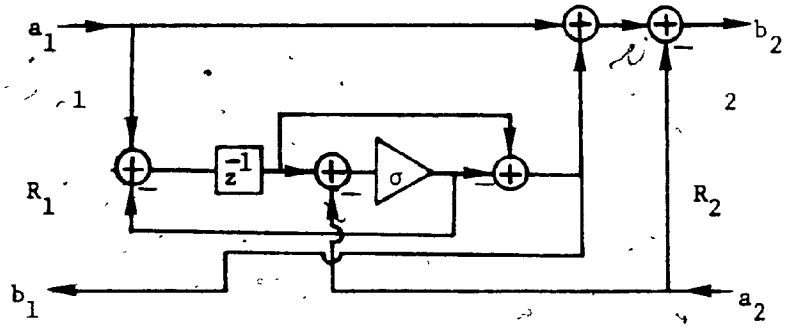
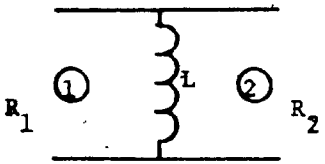
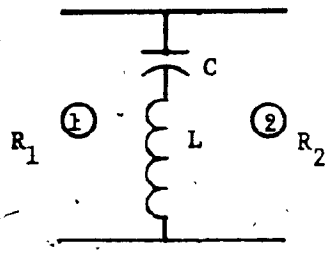
$$[F_p]_T = \begin{bmatrix} \mu_1 & -\lambda_1 \\ -\nu_1 & k_1 \end{bmatrix} \tag{3.45}$$

The realization for the above is the same as that of Z_a with b_1 changed to $-b_1$ and a_2 to $-a_2$. Hence, the realization for the shunt element Y_b may be obtained by starting with the realization of the series element for which $Z_a=Y_b$, transposing it, changing b_1 to $-b_1$, a_2 to $-a_2$ and replacing R_1 by G_1 and R_2 by G_2. Thus, for a shunt capacitor C, the realization is as shown in Table 3.3, where $\sigma=(G_2/G_1)$, $G_1=G_2+C$. Similarly, the realizations for an L and a series LC circuit in the shunt arm can be obtained from that of the corresponding elements in the series arm. These are shown in Table 3.3. It should be observed that there is no delay-free path from a_1 to b_1 in any of these realizations. Thus, any of the networks N_1-N_6 may be cascaded without delay-free loops. It is also seen that if networks N_1-N_6 are used, we may always choose the port resistance R_2 of the last element in the lossless network to be the load resistance R_L. We shall refer to the corresponding digital realization as realization I(a).

We may now obtain an alternate realization for the series element (and hence for the shunt element), and thus obtain an alternate

TABLE 3.3

First Set of Realizations Corresponding to the Shunt Element Y_2 with no Delay-free Path from a_1 to b_1

Element	Corresponding Wave Digital Two-port	Relations
	 Network N_4	$\sigma = \frac{G_2}{G_1}$ $G_1 = G_2+C$
	Same as Network N_4 with z^{-1} replaced by $-z^{-1}$ Network N_5	$\sigma = G_2/G_1$ $G_1 = G_2+1/L$
	Same as Network N_4 with z^{-1} replaced by $g(z^{-1})$ given in (3.19) Network N_6	$\sigma = G_2/G_1$ $G_1 = G_2+\frac{C}{1+LC}$ $\alpha = \frac{1-LC}{1+LC}$

realization for the digital filter.

Consider the series element for which the chain matrix [F] of the corresponding digital two-port N_s is given by (3.21). Let $[F_r]$ be the chain matrix of the two-port obtained by reversing the ports of N_s. Then,

$$[F_r] = \frac{R_2}{R_1} \begin{bmatrix} \mu_1 & -\nu_1 \\ -\lambda & 1 \end{bmatrix} \begin{bmatrix} 1 & k_1 \end{bmatrix} \qquad (3.46)$$

From (3.21) and (3.46), it is seen that $[F_r] = [f]$ if we interchange the roles of R_1 and R_2. Thus, a second realization for Z_a can be obtained by simply reversing the ports of the realizations given in Table 3.1 and interchanging R_1 and R_2 in those realizations. These are shown in Table 3.4. Similarly, a second set of realizations corresponding to Y_2 may be obtained using Table 3.3 and are shown in Table 3.5. It is seen that when these networks are cascaded, there would be no delay-free loops. Further, if these are used in obtaining N for Fig. 3.3, we may always assume that the port resistance R_1 of the first element in the lossless network N to be equal to R_s in Fig. 3.2. We shall refer to the corresponding digital realization as realization II(a).

For the sake of illustration, consider the network of Fig. 3.11. Then, using networks N_1-N_6, we may obtain realizations I(a) and II(a); these are shown in Figs. 3.12 and 3.13. In Fig. 3.12, the different

TABLE 3.4

Second Set of Realizations Corresponding to the Series Element Z_1 with no Delay-free Path from a_2 to b_2

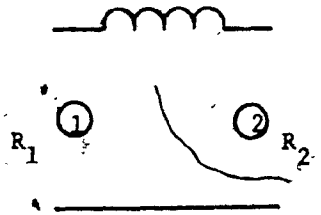
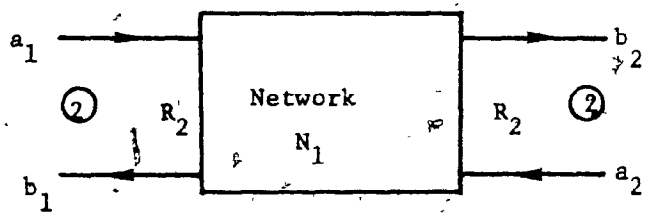
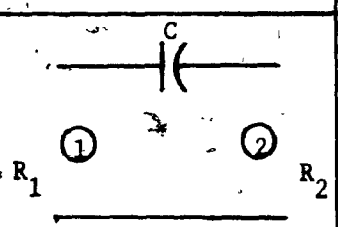
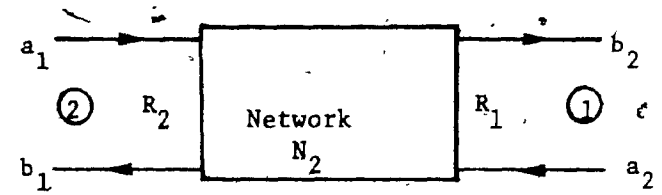
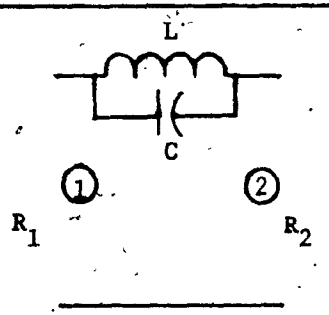
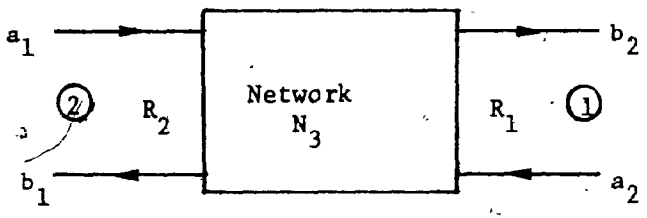
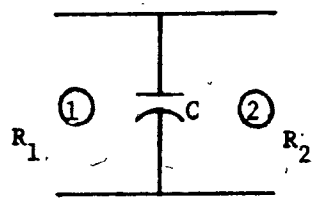
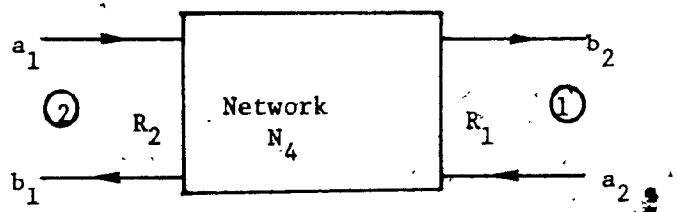
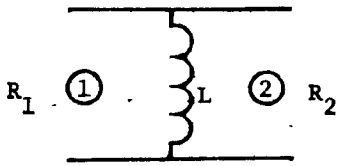
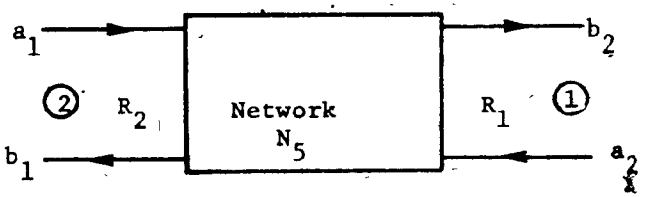
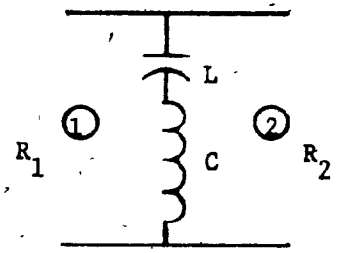
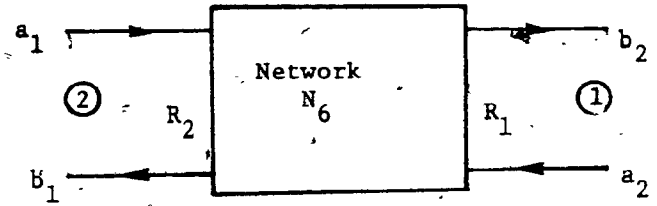
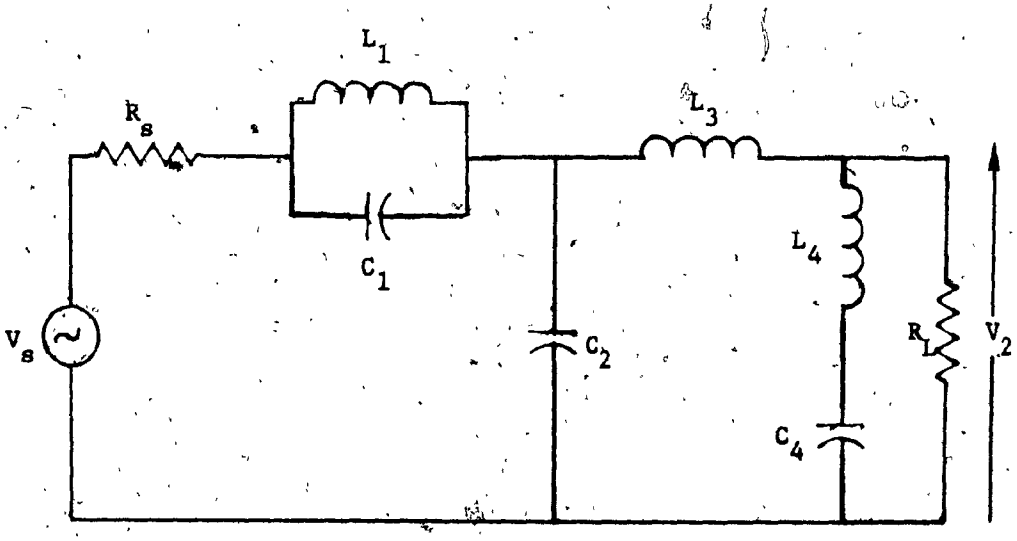
Element	Corresponding Wave Digital Two-port	Relations
		$\sigma = R_1/R_2$ $R_2 = R_1+L$
		$\sigma = R_1/R_2$ $R_2 = R_1+1/C$
		$\sigma = R_1/R_2$ $R_2 = R_1+L/1+LC$ $\alpha=(1-LC)/(1+LC)$

TABLE 3.5

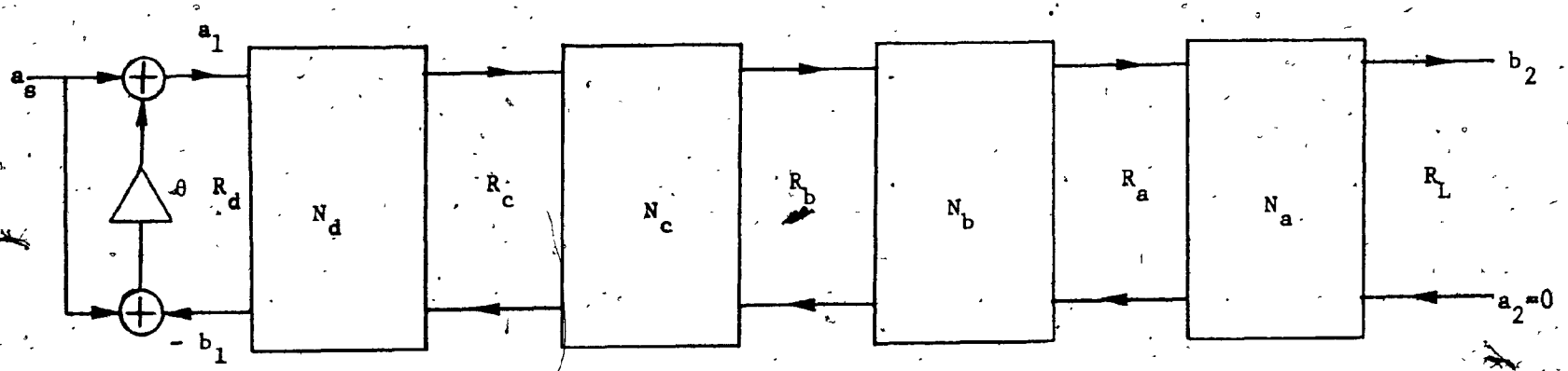
Second Set of Realizations Corresponding to the Shunt Element Y_2 with no Delay-free Path from a_2 to b_2

Element	Corresponding Wave Digital Two-port	Relations
		$\sigma = G_1/G_2$ $G_2 = G_1+C$
		$\sigma = G_1/G_2$ $G_2 = G_1+1/L$
		$\sigma = G_1/G_2$ $G_2 = G_1+C/1+LC$ $\alpha = \frac{1-LC}{1+LC}$



$$T(s) = \frac{V_2}{V_s}$$

FIG. 3.11 - A doubly terminated lossless network of the example in Section 3.5.



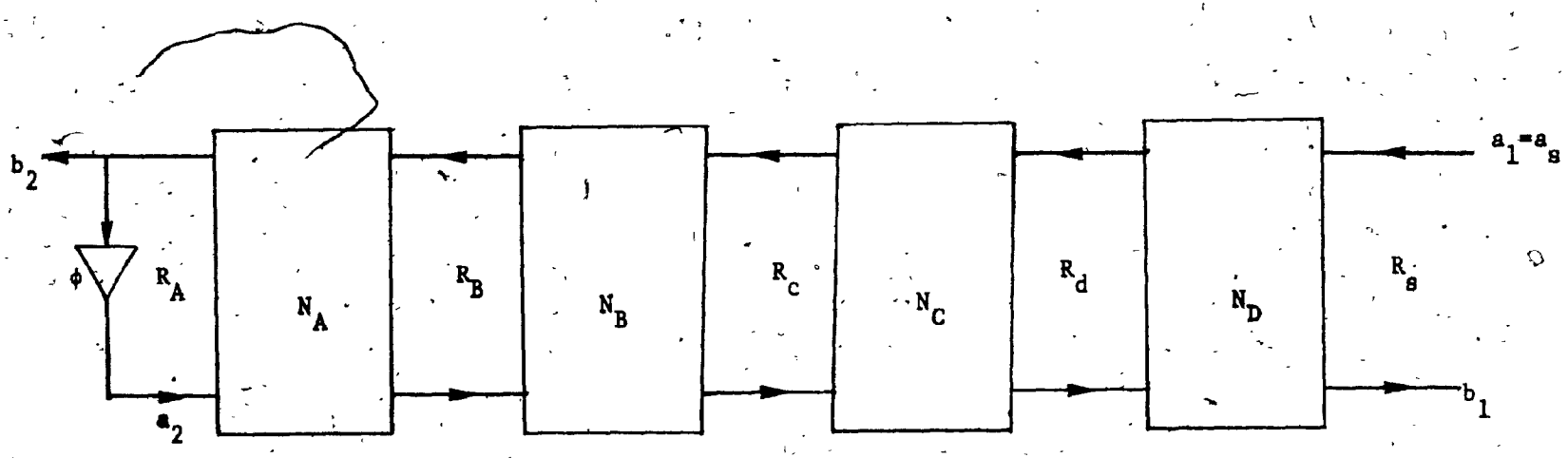
$$G_a = G_L + \frac{C_4}{1+L_4C_4}, \quad R_b = R_a + L_3$$

$$G_c = G_b + C_2, \quad R_d = R_c + \frac{L_1}{1+L_1C_1}$$

$$\theta = (R_d - R_s)/(R_d + R_s)$$

$$\frac{b_2}{a_s} = H_1(z) = 2H(z), \quad a_s = v_s$$

FIG. 3.12 - Type Ia digital structure corresponding to the network of Fig. 3.11.



$$R_D = R_s + \frac{L_1}{1+L_1C_1}\,, \quad G_c = G_D + C_2$$

$$R_B = R_c + L_3\,, \quad G_A = G_B + \frac{C_4}{1+L_4C_4}$$

$$\phi = \frac{R_L - R_A}{R_L + R_A}$$

$$\frac{b_2}{a_s} = H_2(z) = \frac{2}{1+\phi}\,H(z)\,, \quad a_s = v_s$$

FIG. 3.13 - Type IIa digital structure corresponding to the network of Fig. 3.11.

digital two-ports are

$$\begin{aligned} &N_a: \text{ network } N_6 \text{ with } \sigma=G_L/G_a \text{ , } \alpha=(1-L_4C_4)/(1+L_4C_4) \text{ ,} \\ &N_b: \text{ network } N_1 \text{ with } \sigma=R_a/R_b \\ &N_c: \text{ network } N_4 \text{ with } \sigma=G_b/G_c \\ &N_d: \text{ network } N_3 \text{ with } \sigma=R_c/R_d \text{ , } \alpha=(1-L_1C_1)/(1+L_1C_1) \end{aligned} \tag{3.47}$$

and the function realized is

$$\frac{b_2}{a_s} = H_1(z) = 2H(z) \tag{3.48}$$

where

$$H(z) = \frac{v_2}{v_s} \text{ with } s=(z-1)/(z+1) \tag{3.49}$$

In Fig. 3.13, the different networks are

$$\begin{aligned} &N_D: \text{ network } N_3 \text{ with } \sigma=R_s/R_D, \alpha=(1-L_1C_1)/(1+L_1C_1) \text{ ,} \\ &N_C: \text{ network } N_4 \text{ with } \sigma=G_D/G_{c_4} \text{ ,} \\ &N_B: \text{ network } N_1 \text{ with } \sigma=R_c/R_B \text{ ,} \\ &N_A: \text{ network } N_6 \text{ with } \sigma=G_B/G_A \text{ , } \alpha=(1-L_4C_4)/(1+L_4C_4) \text{ ,} \end{aligned} \tag{3.50}$$

and the corresponding function realized is

$$\frac{b_2}{a_1} = H_2(z) = \frac{2}{1+\phi} H(z) \qquad (3.51)$$

with

$$\phi = (R_L - R_4)/(R_L + R_A) \qquad (3.52)$$

3.6 Alternate Canonic Realizations:

We have shown in the previous section that we can always get two canonic realizations for the digital filter of Fig. 3.3, starting with the analog network of Fig. 3.11. In both these realizations, N is a cascade of subnetworks whose chain matrices are of the form (3.7) with $|F| = R_1/R_2$. We have referred to these as realizations I(a) or II(a) depending on whether Tables 3.2 and 3.3 or 3.4 and 3.5 have been used. We shall now show that we can always get three more realizations corresponding to each of I(a) and II(a) [46]. We call these realizations (b), (c) and (d) respectively [46].

Realization (b):

Let the realization (a) [I(a) or II(a)] be as in Fig. 3.3. Let the chain matrix of N be [F] as given by (3.7). Hence, we may express

$$\begin{bmatrix} a_2 \\ b_2 \end{bmatrix} = [F_r] \begin{bmatrix} b_1 \\ a_1 \end{bmatrix} \qquad (3.53)$$

where

$$[F_r] = \frac{R_2}{R_1} \begin{bmatrix} \mu & -\nu \\ -\lambda & k \end{bmatrix} \quad . \tag{3.54}$$

If we now impose the constraints

$$a_1 = -\theta b_1 \tag{3.55a}$$

$$a_2 = (1-\phi)a_s + \phi b_2 \quad , \tag{3.55b}$$

then

$$\frac{b_1}{a_s} = \frac{R_1}{R_2} \frac{(1-\phi)}{\mu + \theta\nu + \phi\lambda + \theta\phi k} \tag{3.56}$$

Using (3.13), (3.20a) and (3.20b), we may reduce (3.56) to

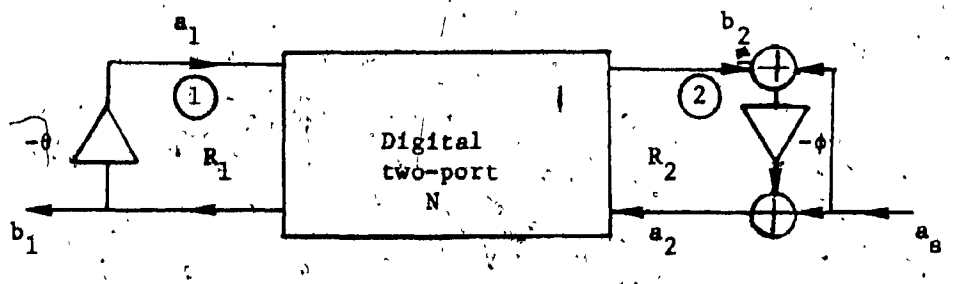
$$\frac{b_1}{a_s} = \frac{R_1}{R_L} \cdot \frac{1}{1+\theta} \, 2H(z) \tag{3.57}$$

The corresponding realization is shown in Fig. 3.14.

Realization (c):

Let N^T be the digital two-port whose transfer matrix is the transpose of that of N. This may be obtained from N by simply reversing the direction of the arrows in N. Then the chain matrix of N^T is

$$[F_T] = \frac{1}{\Delta} [F] \tag{3.58a}$$



$$\frac{b_1}{a_s} = \frac{R_1}{R_L} \frac{1}{1+\theta} 2H(z)$$

FIG. 3.14 - Type Ib or IIb digital realization corresponding to the network of Fig. 3.2.

where

$$\Delta = |F|.$$

If [F] is given by (3.7), then

$$[F_T] = \frac{R_2}{R_1}\begin{bmatrix} \mu & \lambda \\ \nu & k \end{bmatrix} \tag{3.58b}$$

Thus, if N is replaced by N^T in Fig. 3.3, we see that

$$\frac{b_2}{a_s} = \frac{R_1}{R_2}\,\frac{1+\theta}{\mu + \lambda\phi + \nu\theta + k\theta\phi} \tag{3.59}$$

or

$$\frac{b_2}{a_s} = \frac{R_1}{R_2}\,\frac{2}{1+\phi}\,H(z) \tag{3.60}$$

This will be referred to as realization (c) for H(z).

Realization (d):

Similarly, it may be shown that if N is replaced by N^T in Fig. 3.14, we get

$$\frac{b_1}{a_s} = \frac{R_2}{R_L}\,\frac{2}{1+\theta}\,H(z) \tag{3.61}$$

which we will refer to as realization (d) for H(z).

It should be pointed out here that when using type I structures, the multiplier ϕ must be set equal to zero or equivalently R_2 must be set equal to R_L in order to avoid a delay-free loop in the overall structure; setting $R_2=R_L$ results in no loss of generality. Similarly, when using type II structures the multiplier θ must be set equal to zero or equivalently R_1 must be set equal to R_s to avoid a delay-free loop; this again results in no loss of generality.

As an example, let us obtain realizations I(b), I(c), I(d), II(b), II(c) and II(d) from I(a) and II(a) shown in Figs. 3.12, 3.13. These are shown in Figs. 3.15a, b, c, and 3.16a, b and c respectively.

3.7 Conclusions:

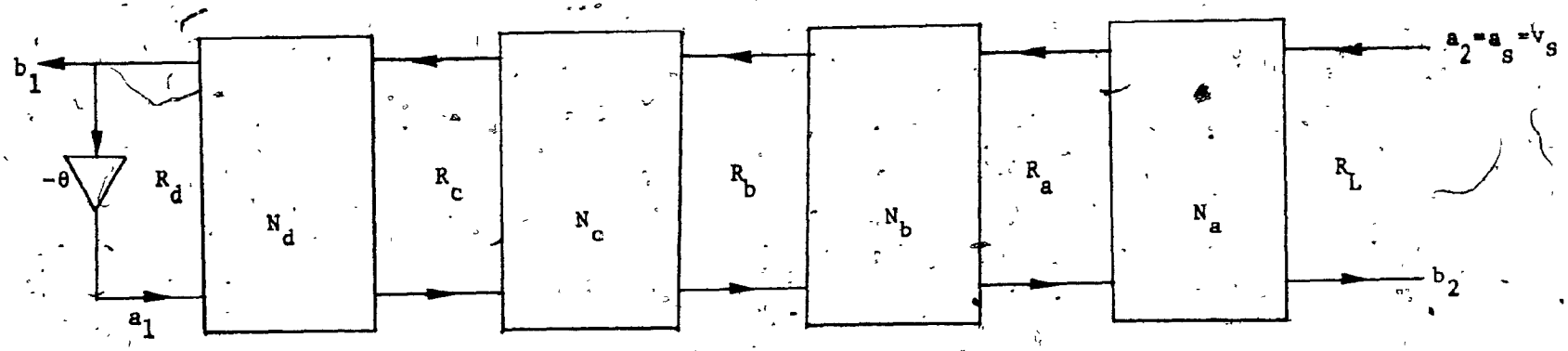
In this chapter, a new type of wave digital filter has been proposed. Doubly terminated lossless ladder networks were considered where the different series and shunt elements were characterized by transfer scattering matrices. Using the bilinear transformation

$$s = (z-1)/(z+1) ,$$

each transfer scattering matrix was transformed to a corresponding chain matrix of a wave digital two-port and the individual two-ports were cascaded to realize the overall chain matrix. The two-port characterization of the analog circuit elements eliminates the need for "adapters" to interconnect the wave two-ports.

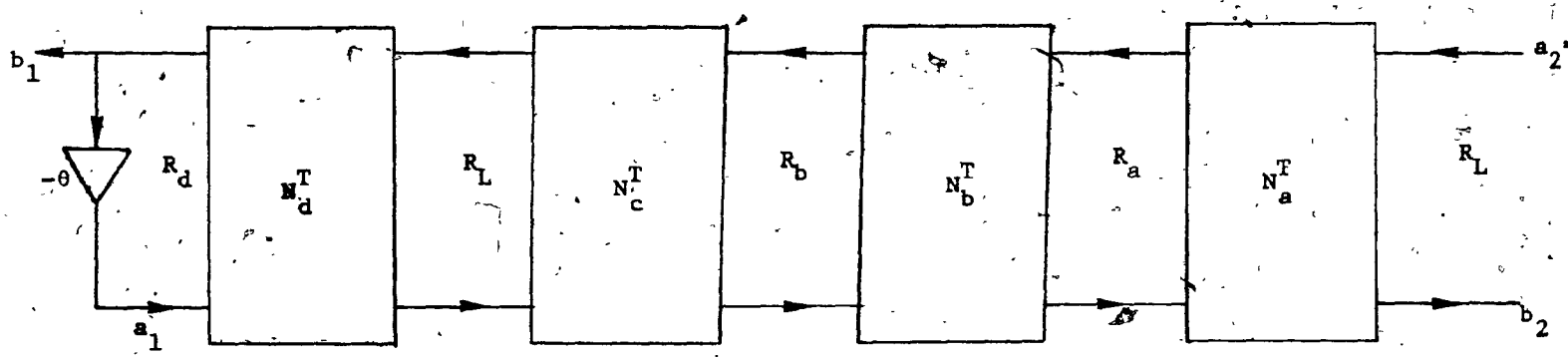
For a given analog structure, it has been shown that one can

obtain eight digital realizations, which are all canonic with respect to both delays and multipliers. The sensitivity properties as well as the round off noise of these different realizations will be dealt with in Chapter V.



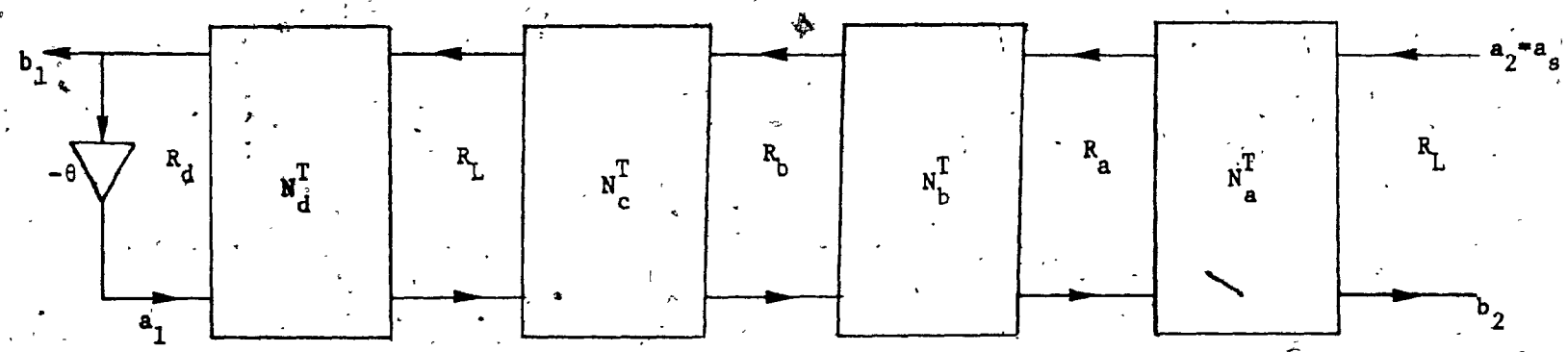
$$\frac{b_1}{a_2} = \frac{R_d}{R_L}\,\frac{1}{1+\theta}\,H_1(z) = \frac{R_d}{R_L}\,\frac{1}{1+\theta}\,2\,.\,H(z)$$

FIG. 3.15a - Type Ib digital structure corresponding to the network of Fig. 3.11.



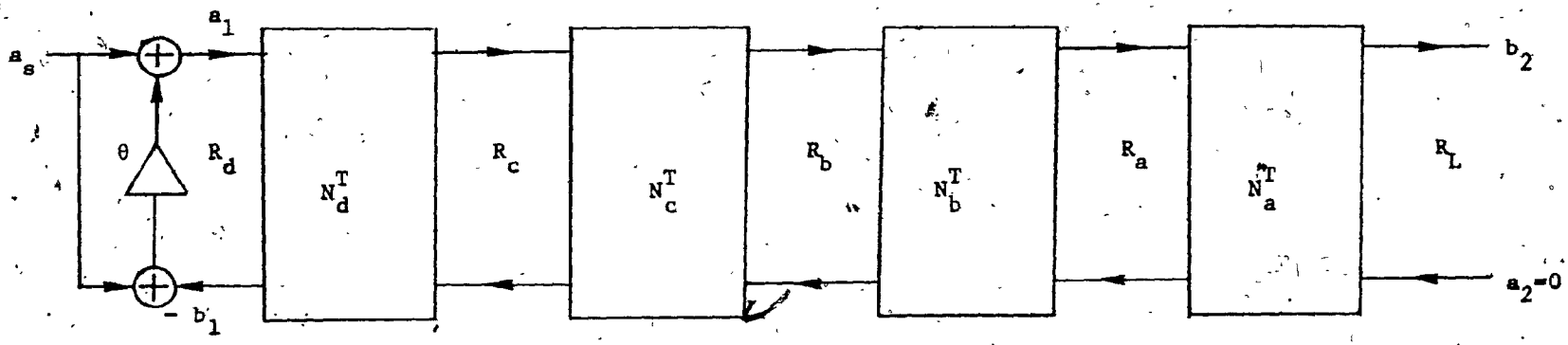
$$\frac{b_1}{a_s} = \frac{1}{1+\theta} H_1(z) = \frac{2}{1+\theta} H(z)$$

FIG. 3.15b - Type Ic digital structure corresponding to the network of Fig. 3.11.



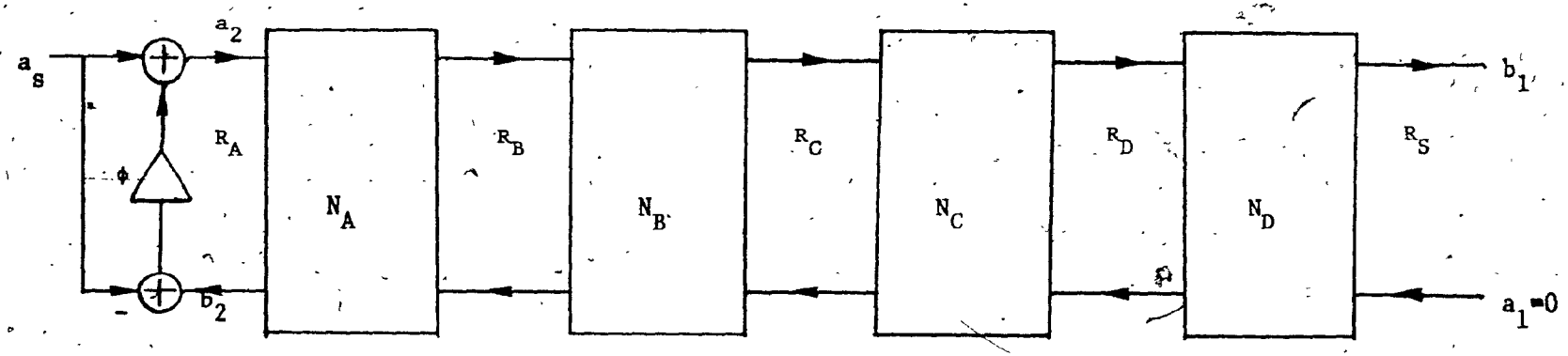
$$\frac{b_1}{a_s} = \frac{1}{1+\theta} H_1(z) = \frac{2}{1+\theta} H(z)$$

FIG. 3.15b - Type Ic digital structure corresponding to the network of Fig. 3.11.



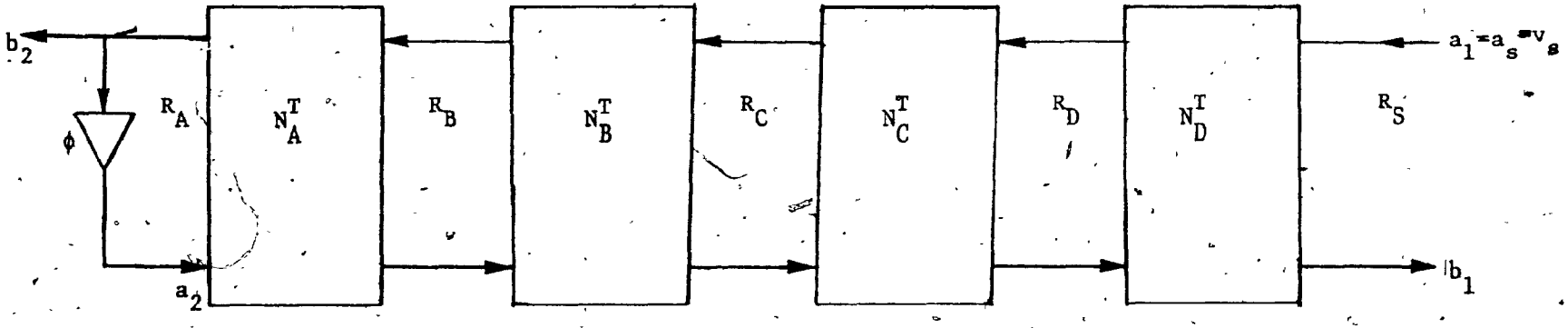
$$\frac{b_2}{a_s} = \frac{R_d}{R_L} H_1(z) = \frac{R_d}{R_L} \; 2\,H(z) \;, \quad a_s = v_s$$

FIG. 3.15c - Type Id digital structure corresponding to the network of Fig. 3.11.



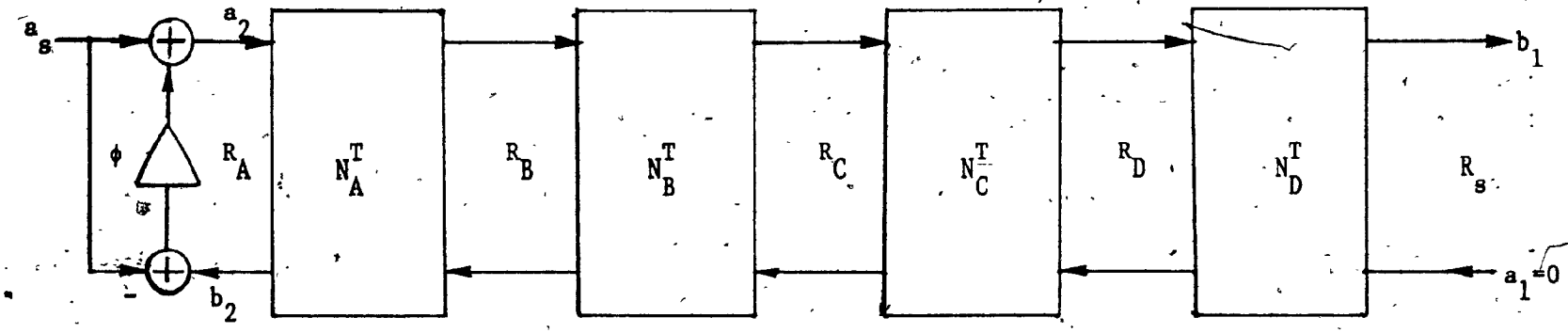
$$\frac{b_1}{a_s} = \frac{R_s}{R_L} \cdot 2\,H(z)\,,\quad a_s = v_s$$

FIG. 3.16a - Type IIb digital structure corresponding to the network of Fig. 3.11.



$$\frac{b_2}{a_s} = \left(\frac{R_S}{R_A}\right) \frac{1}{1+\phi} \quad 2\,H(z).$$

FIG. 3.16b - Type IIc digital structure corresponding to the network of Fig. 3.11.



$$\frac{b_1}{a_s} = \left(\frac{R_A}{R_L}\right) 2\, H(z)$$

FIG. 3.16c - Type IId digital structure corresponding to the network of Fig. 3.11.

CHAPTER 4

BANDPASS AND BANDSTOP WAVE DIGITAL FILTERS WITH VARIABLE CENTER FREQUENCY AND BANDWIDTH

4.1 Introduction:

Wave digital filters realized by Fettweis' method [13,31-28] have been shown to possess good sensitivity properties compared to the conventional realizations. In a later chapter we will show that the wave digital realizations proposed in chapter 3 also possess good sensitivity properties. In Fettweis' method, each analog element is characterized by a wave digital one-port and a digital filter is obtained, in principle, by interconnecting these wave digital one-ports with the appropriate adapters. The method proposed in chapter 3, on the other hand, depends on wave digital two-port descriptions for the analog elements. The overall digital filter is obtained by cascading the individual wave two-ports. The discussion in this chapter relates to the wave digital filters proposed in the previous chapter.

In order to obtain a bandpass (BP) or a bandstop (BS) digital filter, we can start with a prototype lowpass (LP) analog filter, then obtain the appropriate BP or BS analog filter and then obtain the corresponding wave digital filter. This method suffers from the fact that the center frequency and bandwidth cannot be independently controlled by varying the multiplier values. On the other hand, we can realize a BP or BS wave digital filter using the spectral transformations given

4.4 Conclusions:

It is shown that by a proper rearrangement of the BP or BS transformation in the analog domain, the center frequency and BW can be controlled independently in the resulting wave digital filter. It is further shown that the multiplier which controls the center frequency is the same for all the sections in the BP or BS wave digital filter structure and hence a saving in coefficient register is achieved.

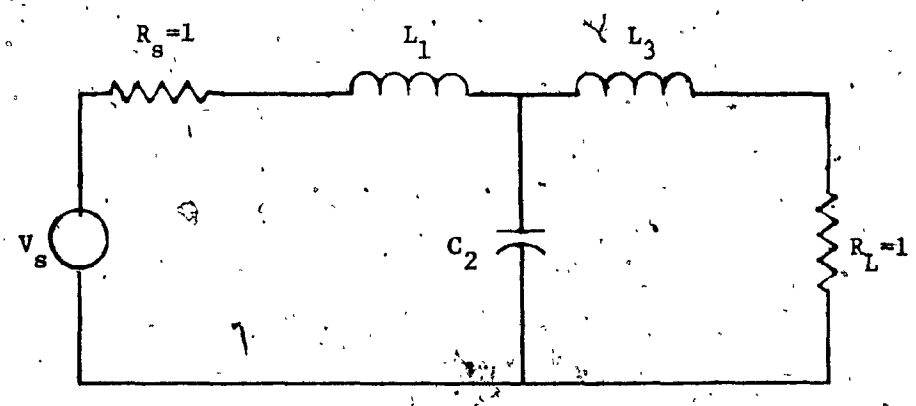


FIG. 4.1 - A prototype LP filter for the example in Section 4.3.

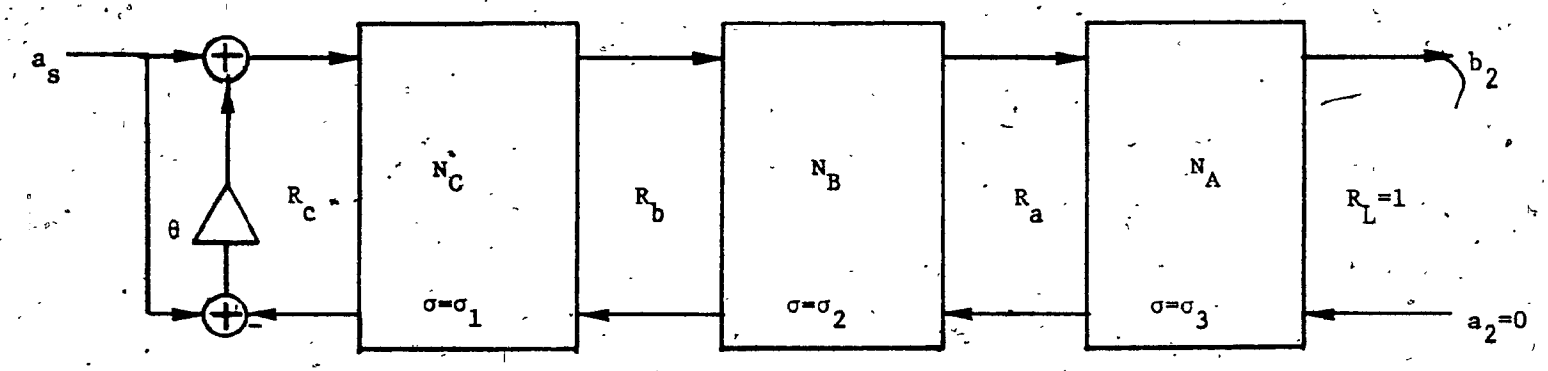
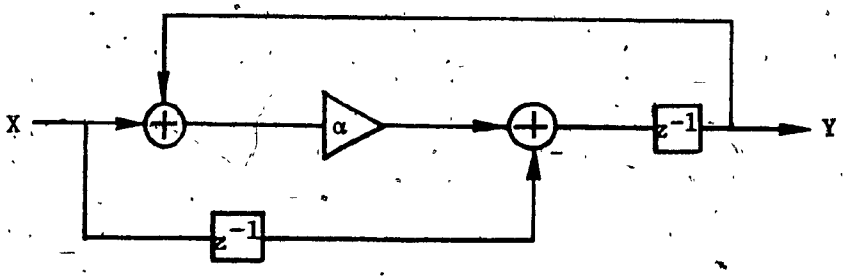


FIG. 4.2 - The prototype wave digital filter corresponding to the network in Fig. 4.1.,



$$\frac{Y}{X} = g(z^{-1}) = -\frac{z^{-1}(z^{-1}-\alpha)}{1-\alpha z^{-1}}$$

FIG. 4.3 - A digital realization for $g(z^{-1})$ in equation (4.13).

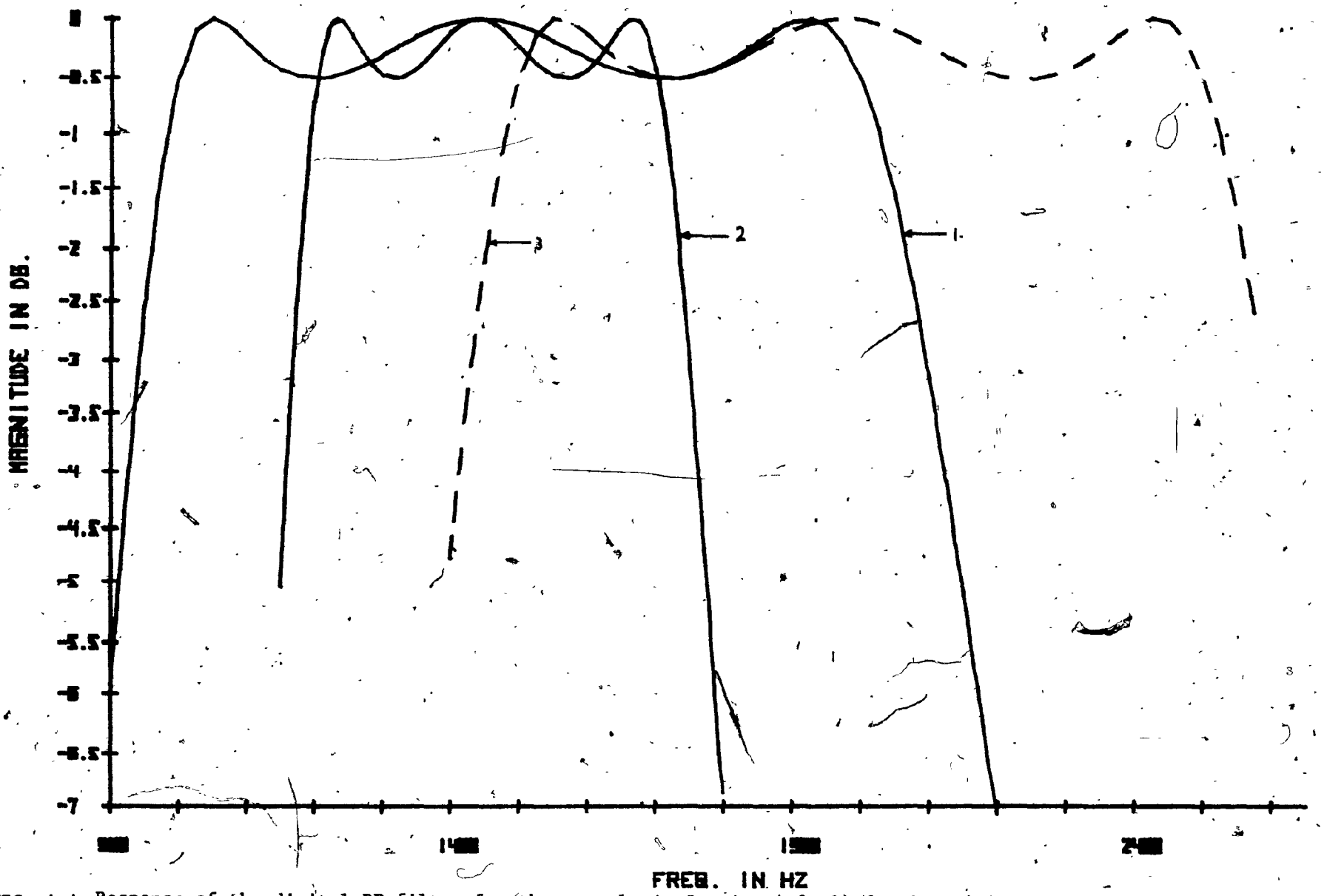


FIG. 4.4- Response of the digital BP filter for the example in Section 4.3; 1) for Ω_0=1.414 KHz, BW=1 KHz, 2) for Ω_0=1.414 KHz BW=500 Hz, 3) for Ω_0=1.937 KHz, BW=1 KHz.

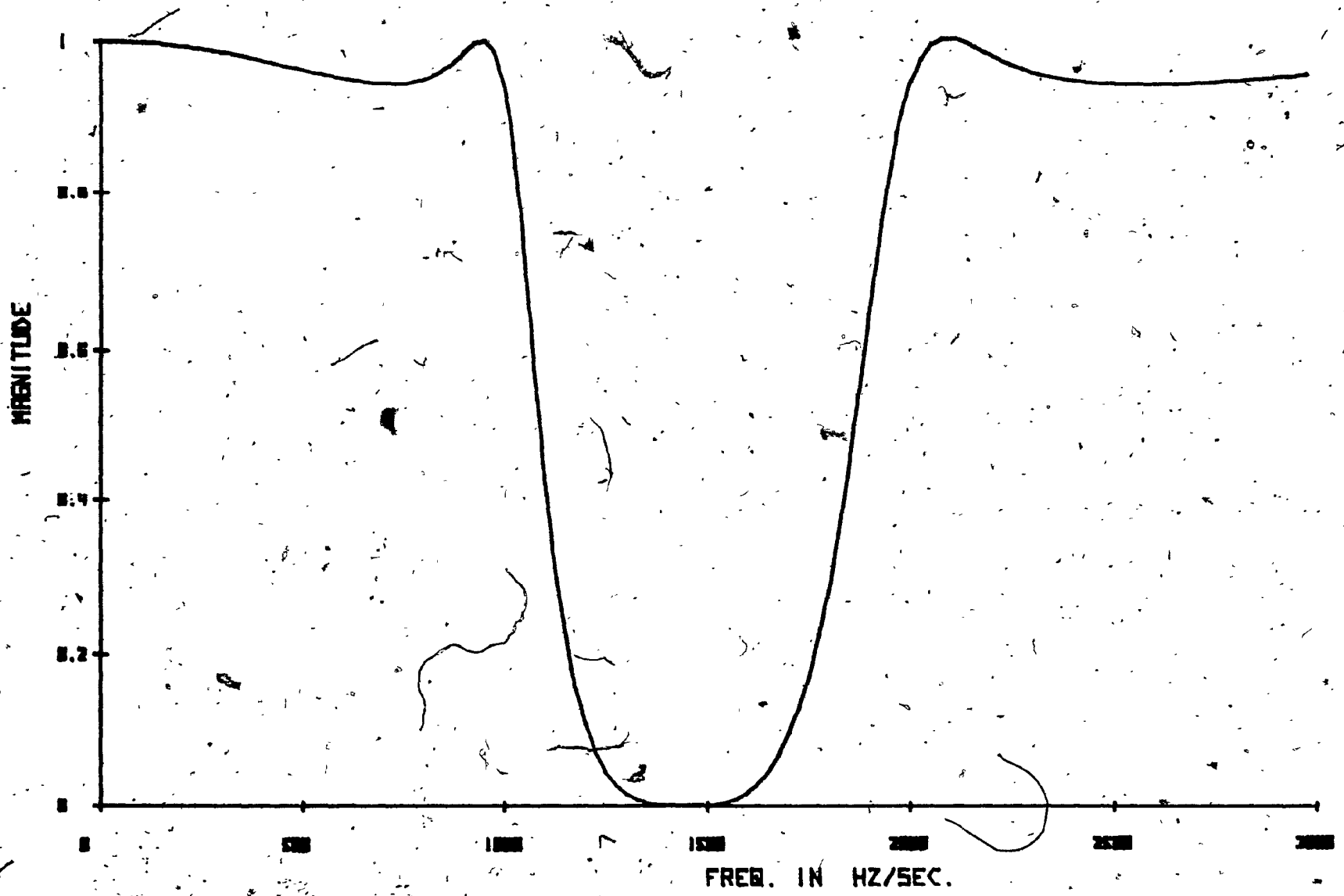


FIG. 4.5 - Response of the BS digital filter for the example in Section 4.3 for Ω_0=1.414 KHz and BW=500 Hz.

CHAPTER 5

COEFFICIENT SENSITIVITY AND ROUNDOFF NOISE ANALYSIS

5.1 Introduction:

With the advent of LSI techniques and with the microprocessors entering the market, there has been greater emphasis on the construction of special purpose hardware for real-time digital filtering applications. The cost of such hardware depends directly on factors such as the required data and coefficient word lengths, scaling requirements and the number of arithmetic operations required per sample. These factors are, in turn, strongly influenced by the choice of a network structure that is used for the implementation. Consequently there has been great interest recently in the design and analysis of different types of structures with the view that some of them might be most suitable from the point of view of hardware considerations.

When a digital filter is implemented by means of a special-purpose hardware the coefficient and signal wordlengths are both finite. Due to finite coefficient accuracy, the given transfer function can not be realized exactly. As a result, there will be a shift in the frequency characteristics (like the dc gain, cutoff frequency etc.) from the specified ones. This is usually known as the sensitivity of the filter due to coefficient rounding. The shorter signal (or data) wordlength limits the accuracy of arithmetic operations and in effect introduces a noise at the output. This is known as the roundoff noise associated with a digital filter.

In this chapter we shall carry out the floating-point sensitivity and roundoff error associated with the wave digital structures proposed in Chapter 3. The results on floating-point coefficient sensitivity and roundoff noise in Fettweis' wave digital structures are already available in [60]. Hence, we shall use these results reported in [60] to compare the sensitivity and roundoff error in the digital realizations proposed in the 3rd Chapter with those of Fettweis' structures and the conventional realizations.

Section 5.2 contains the floating-point coefficient sensitivity and Section 5.3 the roundoff noise in the digital structures that were proposed earlier in Chapter 3.

5.2 Coefficient Sensitivity:

In order to compare the coefficient sensitivity of different digital structures Ku and Ng [60] have used a root mean square (rms) error in the frequency response given by

$$E_{rms} = \left[\frac{1}{N+1} \sum_{i=0}^{N} W(\Omega_i) \, [\Delta H(\Omega_i)]^2 \right]^{\frac{1}{2}} \qquad (5.1)$$

where N is the number of equally spaced frequency points in the filter passband, ΔH is the difference between the magnitudes of the frequency response of the ideal filter (with infinite coefficient accuracy) and of the filter with its multiplier coefficient values rounded, and W is a weighting function. The weighting function accentuates the relative importance of error in the frequency response in different frequency bands. In our study, the weighting function is set equal to unity since

we are mainly interested in the passband [60]. The E_{rms} in (5.1) is the basis of comparison of the coefficient sensitivities associated with various digital structures. The mantissa part of a floating-point number is rounded to a specified length in sign magnitude representation. However, the wordlength requirements of the sign and exponent are not counted. The magnitude of the frequency response is always normalized to unity at zero frequency (since only lowpass filters are considered) to compensate for the constant gain shifts in the passband.

Two cases are considered: (i) a second-order lowpass Butterworth filter and (ii) a seventh-order lowpass Chebyshev filter having 1 db passband ripple. In each case a wave digital structure is derived from a corresponding doubly terminated LC ladder network using the method outlined in Chapter 3, and the E_{rms} in (5.1) computed. The values of N in (5.1) are taken as 50 and 100 respectively for the second-order and the seventh-order filters. Since it is known that the sensitivity deteriorates with decreasing filter bandwidth (or increasing sampling frequency) and coefficient wordlength, these two parameters are varied in computing the E_{rms} in (5.1). A normalized filter bandwidth f_n, as defined by

$$f_n = f_c/f_s \tag{5.2}$$

is used, where f_c is the actual filter cutoff frequency and f_s is the sampling frequency. In order to account for the varying bandwidth, the L's and C's in the reference analog network are frequency scaled using

$$L = L'/\tan(\pi f_n)$$
$$C = C'/\tan(\pi f_n) \qquad (5.3)$$

where L' and C' are the values corresponding to the unity bandwidth case.

(i) Second-order Filter:

A second-order analog lowpass Butterworth filter and its corresponding wave digital filter derived using the method proposed in the 3rd Chapter are shown in Figs. 5.1 and 5.2 respectively. The sensitivity measure as defined in (5.1) is computed for the structure in Fig. 5.2 using N=50. Figs. 5.3a and b show the E_{rms} vs. the normalized bandwidth for coefficient wordlengths of 8 and 12 bits respectively. The same figs. also show the E_{rms} for Fettweis' new structure and the direct realization as found in [60]. At a large relative bandwidth all the three types of realizations have more or less the same rms error in the frequency response as expected, but at narrow bandwidths the rms error for the direct realization increases while it does not increase for the wave digital structure proposed in the 3rd Chapter and Fettweis' new structure. The complexity of these structures are shown in Table 5.1.

(ii) Seventh-order Filter:

A seventh-order lowpass analog network of the Chebyshev type with 1 db passband ripple is shown in Fig. 5.4. The corresponding type I

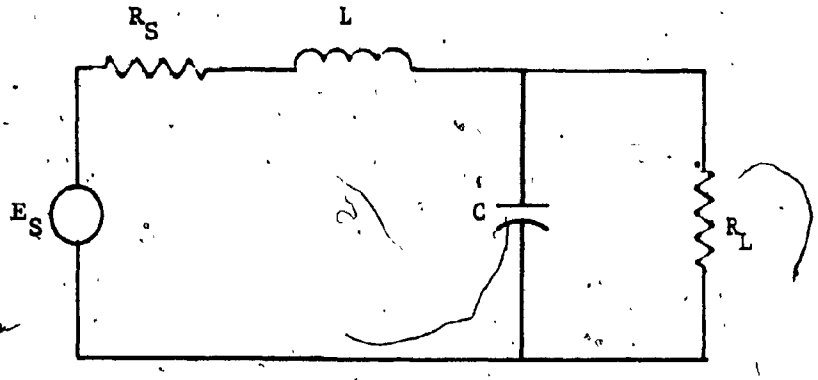


FIG. 5.1 - Second-order Prototype LC Ladder Network.

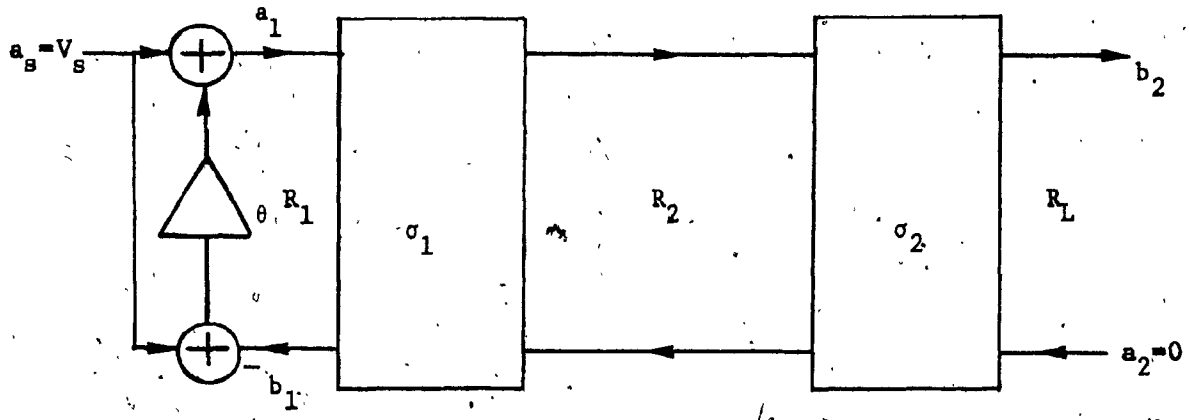


FIG. 5.2 - Proposed Wave Digital Realization Corresponding to Fig. 5.2.

$$G_2 = C + \frac{1}{R_L} \qquad \theta = \frac{R_1 - R_s}{R_1 + R_s}$$

$$R_1 = L + \frac{1}{G_2}$$

$$\sigma_2 = \frac{G_L}{G_2}$$

$$\sigma_1 = \frac{R_2}{R_1}$$

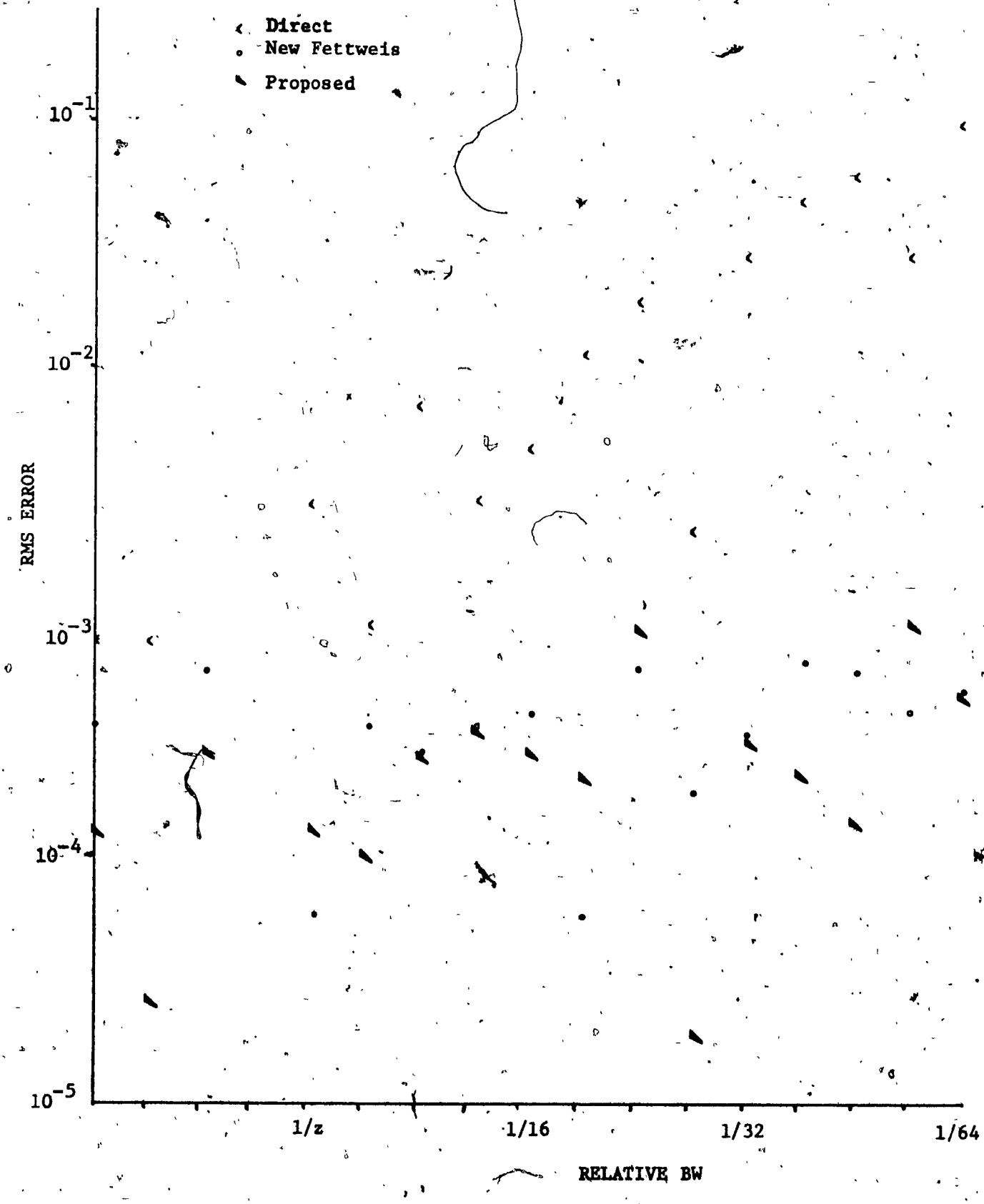


FIG. 5.3a - The RMS Error in Frequency Response versus Bandwidth for Second-order Digital Filters for Coefficient Wordlengths of 8 bits.

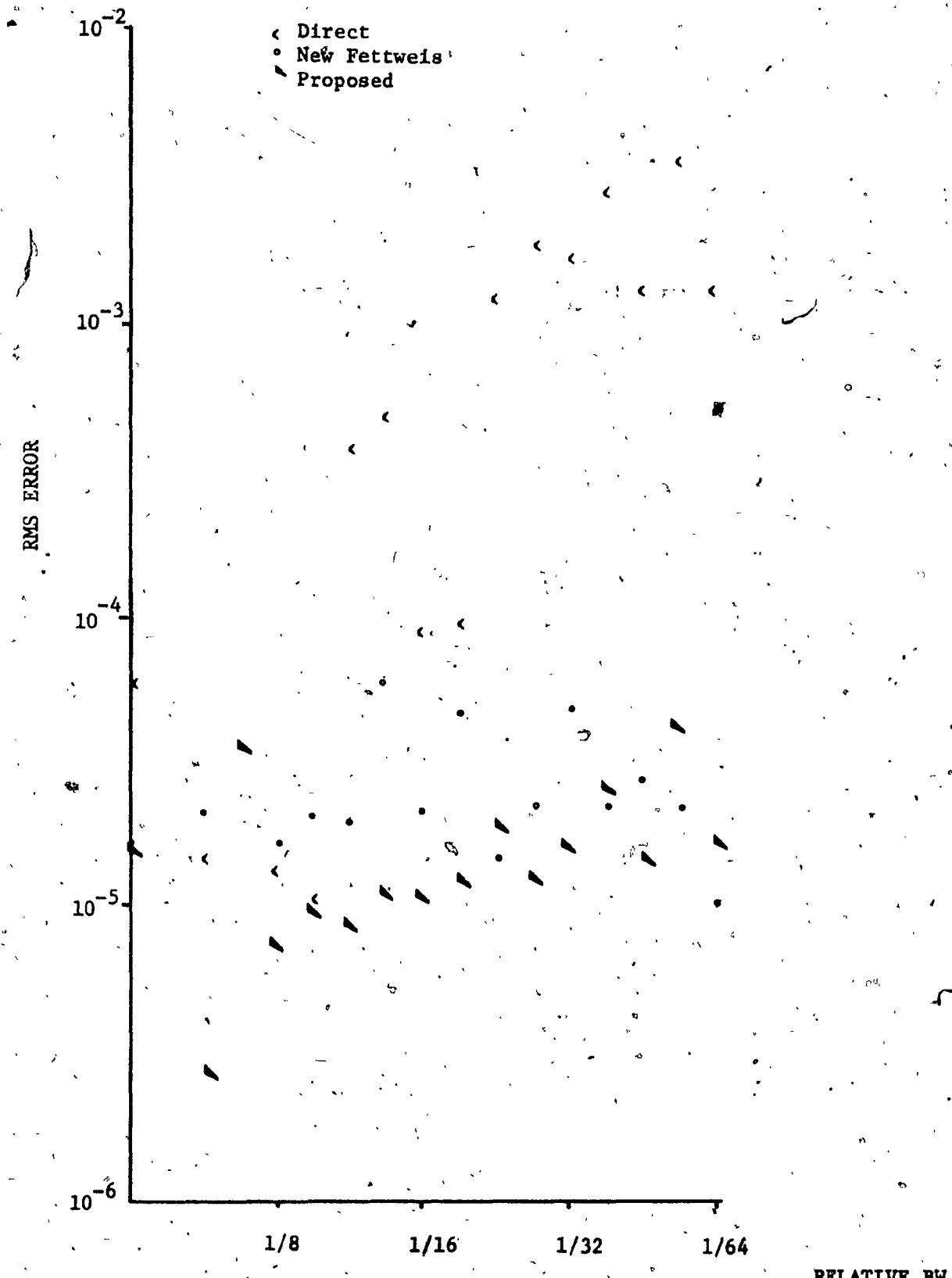


FIG. 5.3b – The RMS Error in Frequency Response versus Bandwidth for Second-order Digital Filters for Coefficient Wordlengths of 12 bits.

TABLE 5.1

Complexity of 2nd-order Digital Filter Structures

Structure	# of Delays	# of Multi-plications	# of Additions	# of Coeffts. Stored
Direct Form	2	2	4	2
Fettweis (new)	2	3	11	2*
Proposed	2	3	10	3

* due to symmetry.

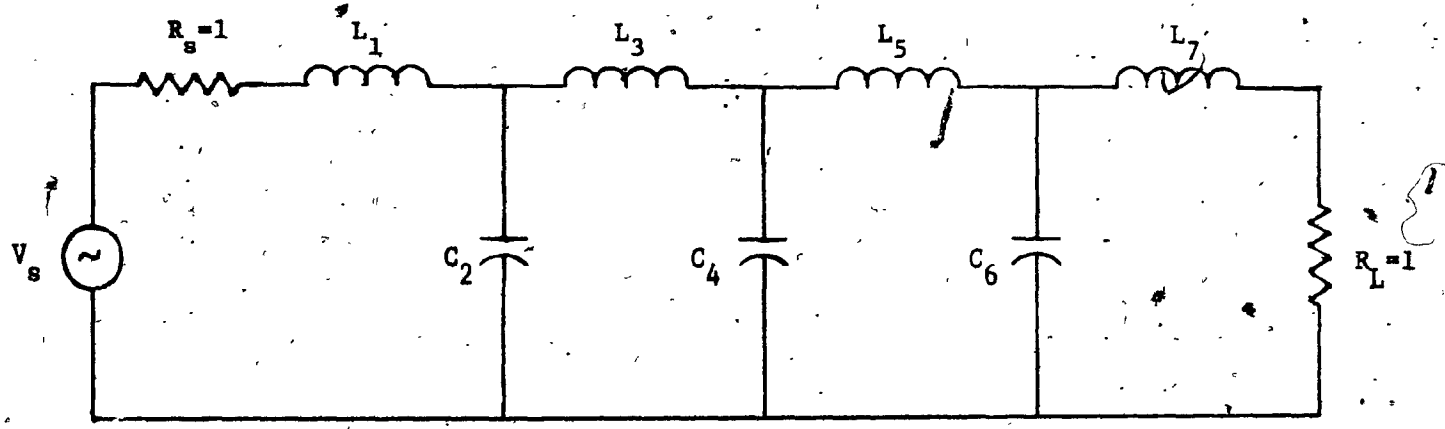


FIG. 5.4 - Doubly Terminated Seventh-order Lowpass LC Ladder Network.

and II wave digital realizations [46] are shown in Figs. 5 and 6 respectively. The port normalization constants and the multiplier values for type I structures are determined [46] by

$$\begin{aligned} R_7 &= R_L + L_7 \\ G_6 &= C_6 + 1/R_7 \\ R_5 &= L_5 + 1/G_6 \\ G_4 &= C_4 + 1/R_5 \\ R_3 &= L_3 + 1/G_4 \\ G_2 &= C_2 + 1/R_3 \\ R_1 &= L_1 + 1/G_2 \end{aligned} \tag{5.4}$$

and

$$\begin{aligned} \sigma_7 &= R_L/R_7 \\ \sigma_6 &= 1/(G_6 R_7) \\ \sigma_5 &= 1/(R_5 G_6) \\ \sigma_4 &= 1/(G_4 R_5) \\ \sigma_3 &= 1/(R_3 G_4) \\ \sigma_2 &= 1/(G_2 R_3) \\ \sigma_1 &= 1/(R_1 G_2) \\ \theta &= (R_1 - R_s)/(R_1 + R_s) \end{aligned} \tag{5.5}$$

while those for type II structures are determined [46] by

$$
\begin{aligned}
R_7 &= R_s+L_1 \\
G_6 &= C_2+1/R_7 \\
R_5 &= L_3+1/G_6 \\
G_4 &= C_4+1/R_5 \\
R_3 &= L_5+1/G_4 \\
G_2 &= C_6+1/R_3 \\
R_1 &= L_7+1/G_2
\end{aligned}
\qquad (5.6)
$$

and

$$
\begin{aligned}
\sigma_1 &= R_s/R_7 \\
\sigma_2 &= 1/(G_6R_2) \\
\sigma_3 &= 1/(R_5G_6) \\
\sigma_4 &= 1/(G_4R_5) \\
\sigma_5 &= 1/(R_3G_4) \\
\sigma_6 &= 1/(G_2R_3) \\
\sigma_7 &= 1/(R_1G_2), \phi = (R_L-R_1)/(R_L+R_1)
\end{aligned}
\qquad (5.7)
$$

The sensitivity measure as defined in (5.1) is computed for the realizations in Figs. 5.5 and 5.6 in the same way as was done for the second-order case except that a value of 100 is used for N. In Figs. 5.7a and b are shown the E_{rms} vs. the coefficient wordlengths for relative bandwidths of 1/4 and 1/16 for the wave digital filters proposed in the 3rd chapter. The same figures also show the E_{rms} for the Fettweis' new structure and

the conventional cascade realization [60]. Fig. 5.8 shows the E_{rms} as a function of the relative bandwidth for a coefficient wordlength of 10 bits for all the three types of realizations.

At a large relative bandwidth of 1/4 all the three different realizations have more or less the same rms error in the frequency response as expected. However, at very narrow bandwidths, the rms error increases rapidly for the conventional cascade realization while it is fairly constant for the digital structures proposed in Chapter 3 and Fettweis' new structure. The complexity of the various digital structures is shown in Table 5.2.

It is well-known that the poles (and zeros) of a digital filter move close to the unit circle in the z-plane as the sampling frequency is increased. As a consequence the frequency response error increases rapidly in the case of conventional realizations [38]. Also, with decreasing coefficient wordlength the frequency response error increases, as one might expect.

However, there is not much increase in the rms error in the frequency response for Fettweis' new structure and the structures proposed in the 3rd chapter, when bandwidth and coefficient wordlengths are decreased. Following [60] this may be explained as follows: First, the rounded multiplier coefficients in the wave digital structures determine a new set of element values in the corresponding analog reference network as determined by the equations (5.4) and (5.5) or (5.6) and (5.7). These new analog element values are, of course, different from the ideal ones. The amount of change in the analog element values, however, depends on

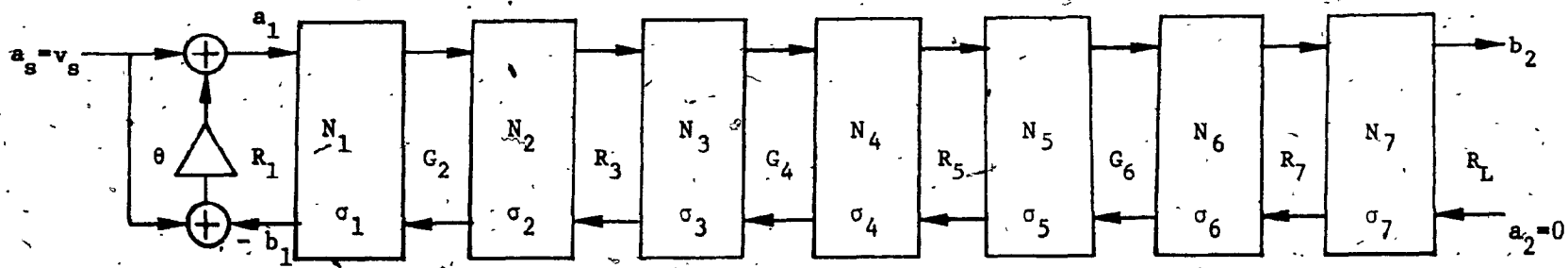


FIG. 5.5a – Type Ia Wave Digital Structure Corresponding to the Network of Fig. 5.4.

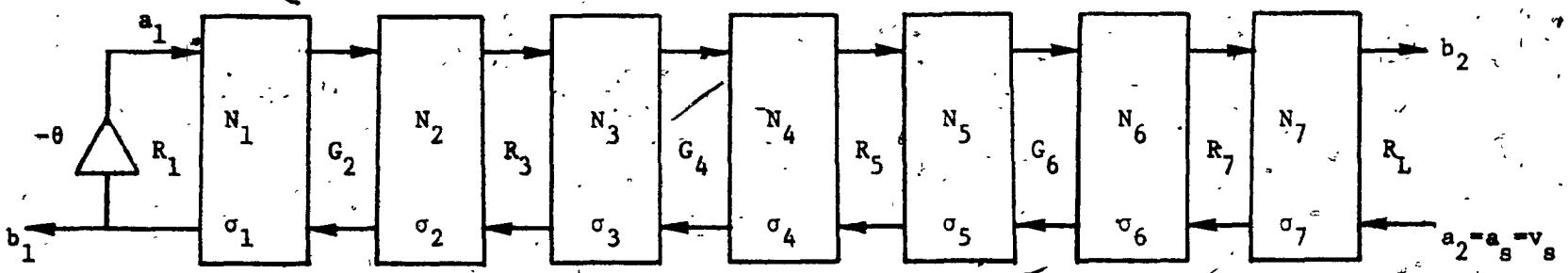


FIG. 5.5b - Type Ib Wave Digital Structure Corresponding to the Network of Fig. 5.4.

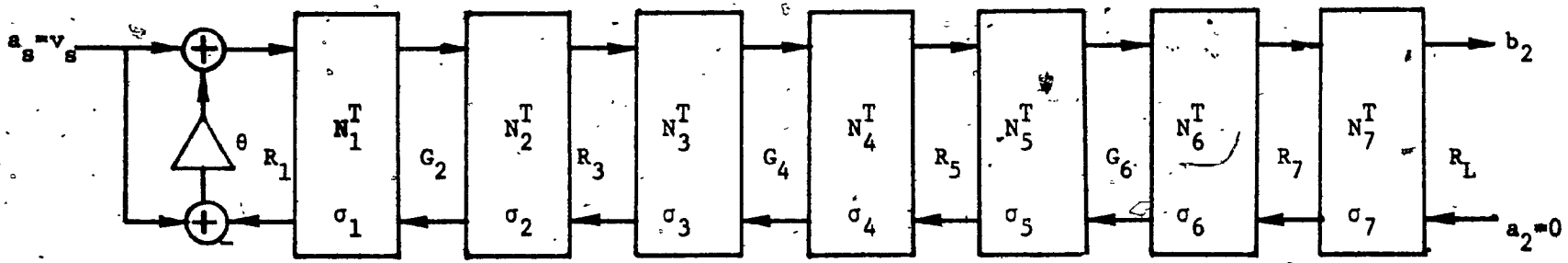


FIG. 5.5c - Type Ic Wave Digital Structure Corresponding to the Network of Fig. 5.4.

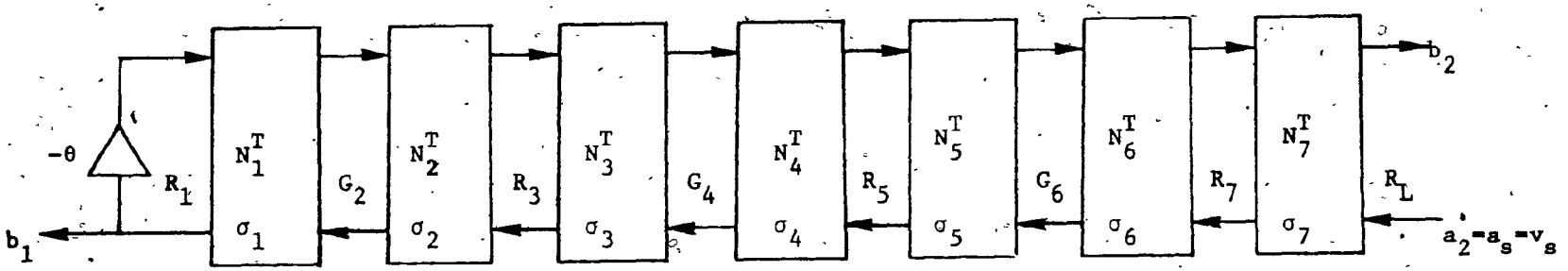


FIG. 5.5d - Type Id Wave Digital Structure Corresponding to the Network of Fig. 5.4.

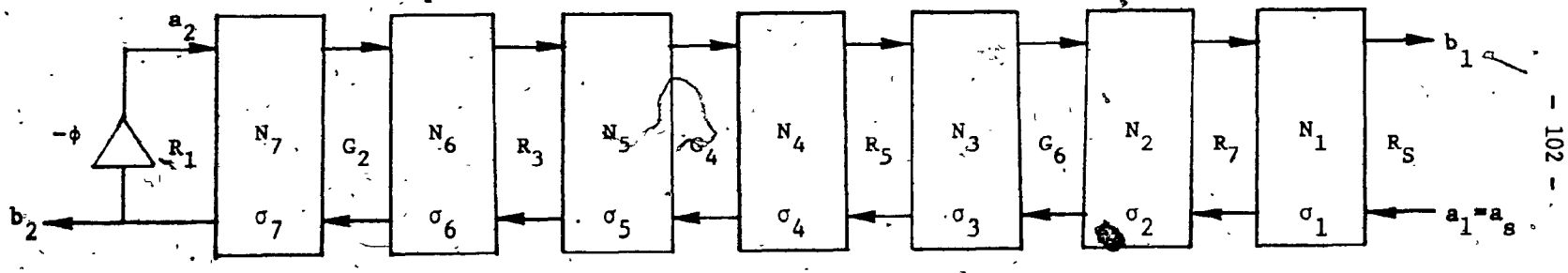


FIG. 5.6a - Type IIa Wave Digital Structure Corresponding to the Network of Fig. 5.4.

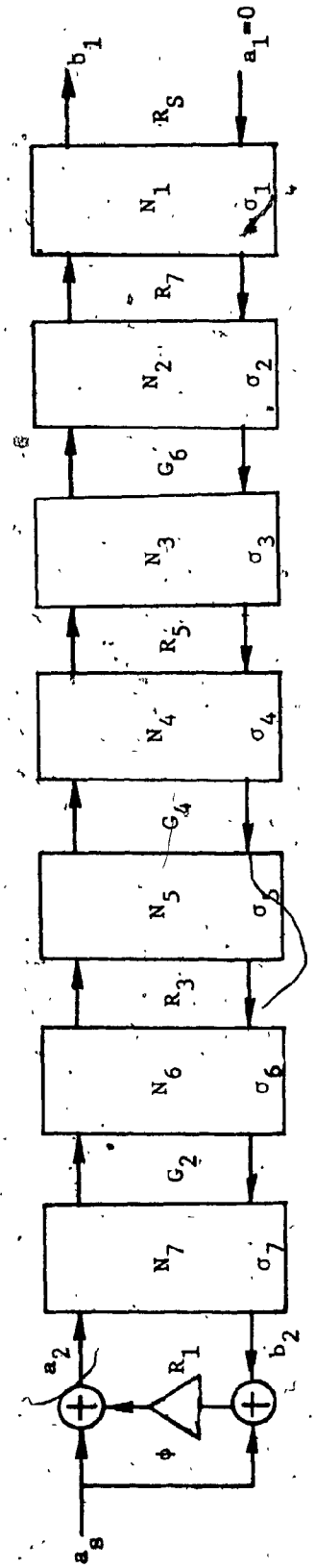


FIG. 5.6b - Type IIb Wave Digital Structure Corresponding to the Network of Fig. 5.4.

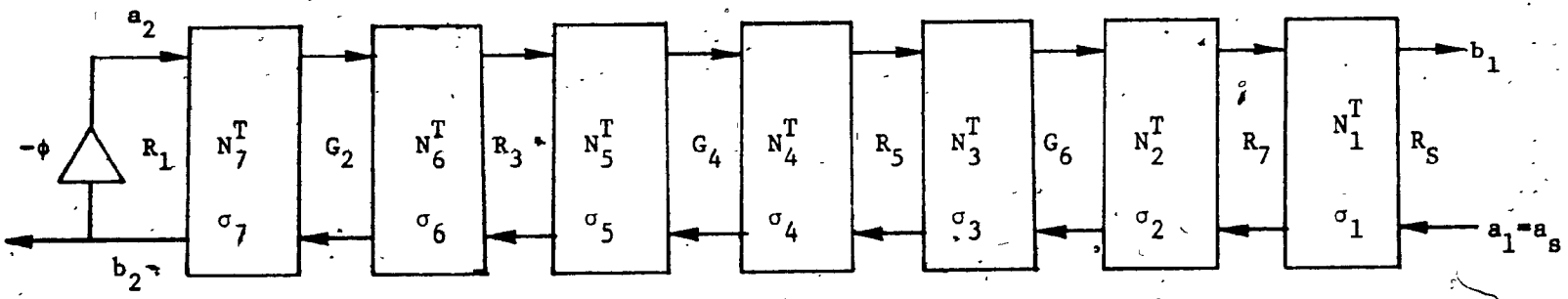


FIG. 5.6c - Type IIc Wave Digital Structure Corresponding to the Network of Fig. 5.4.

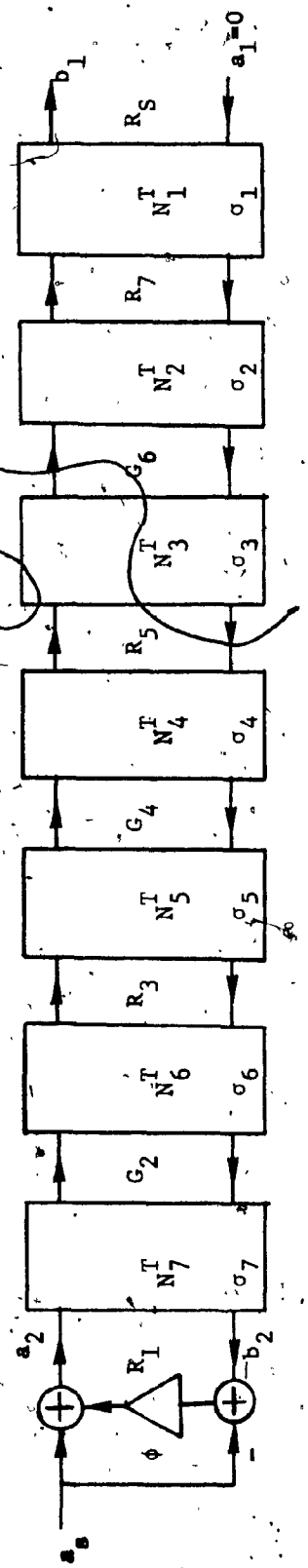


FIG. 5.6d - Type IId Wave Digital Structure Corresponding to the Network of Fig. 5.4.

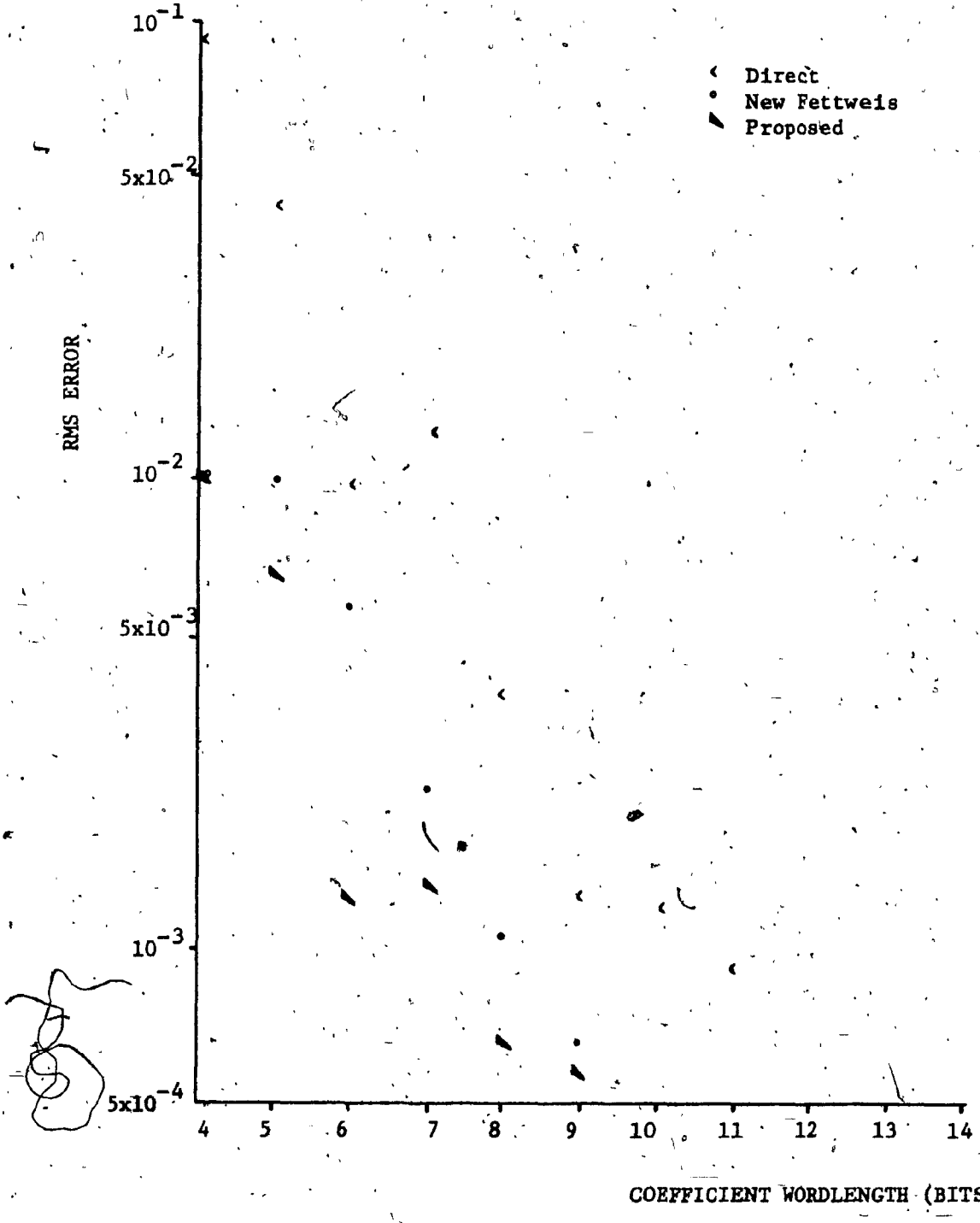


FIG. 5.7a - The RMS Error in Frequency Response versus Coefficient Wordlength for Seventh-order Digital Filters for a Relative Bandwidth of 1/4.

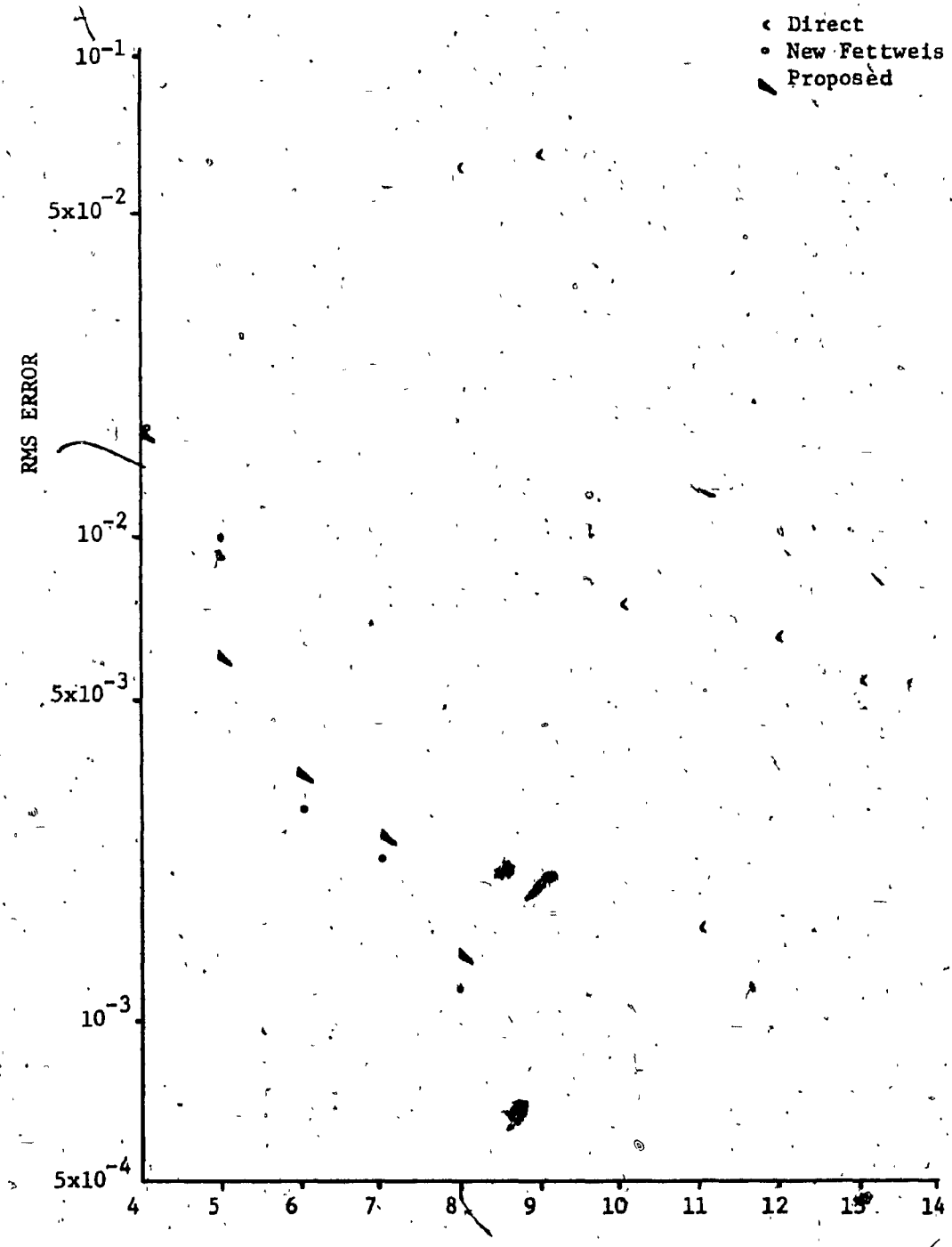


FIG. 5.7b - The RMS Error in Frequency Response versus Coefficient Wordlength for Seventh-order Digital Filters for a Relative Bandwidth of 1/16.

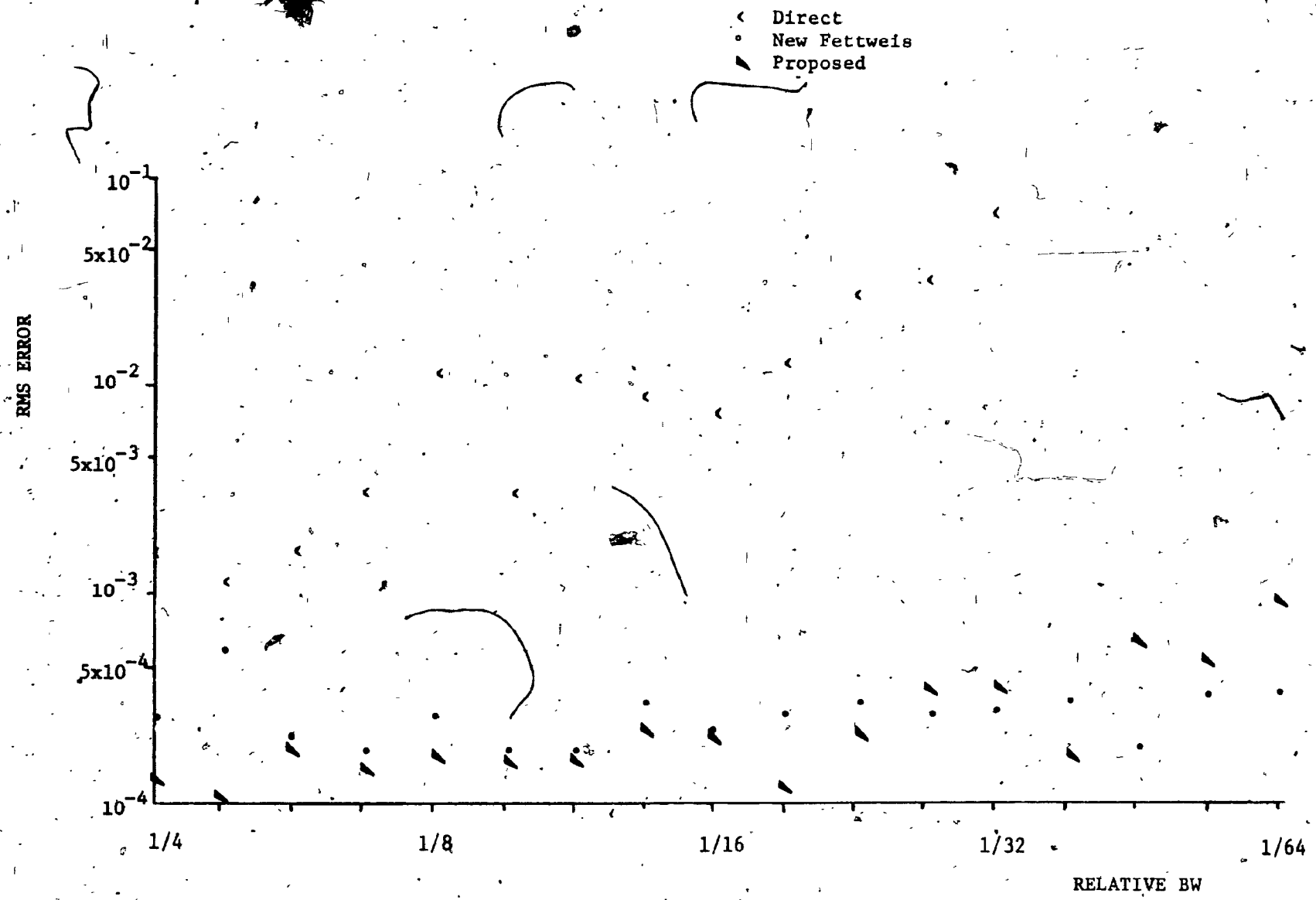


FIG. 5.8 - The RMS Error in Freqdency Response versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Wordlengths of 10 bits.

TABLE 5.2

Complexity of 7th-order Digital Filter Structures

Structure	# of Delays	# of Multiplications	# of Additions	# of Coeffts. Stored
Cascade	7	7	14	7
Fettweis (new)	7	7	28	4*
Proposed				
Ia	7	8	34	8
Ib	7	8	34	8
Ic	7	8	35	8
Id	7	8	34	8
IIa	7	8	34	8
IIb	7	8	34	8
IIc	7	8	34	8
IId	7	8	35	8

* due to symmetry.

TABLE 5.3

% Change in the Prototype Element Values due to Rounding of Multiplier Coefficients

Relative BW=1/4

Coefficient Wordlength (Bits)	L_1	% Change	L_3	% Change	L_5	% Change	L_7	% Change	C_2	% Change	C_4	% Change	C_6	% Change
∞	2.1666	-	3.0936	-	3.0936	-	2.1666	-	1.1115	-	1.1735	-	1.1115	-
4	2.1	-3.0739	3.0333	-1.9481	3.0333	-1.9481	2.2	1.5416	1.1607	4.4277	1.1607	-1.0895	1.1161	0.4113
6	2.2285	2.8550	3.1684	2.4163	3.1684	2.4163	2.2	1.5416	1.0885	-2.0650	1.1458	-2.3576	1.0910	-1.8436
8	2.1572	-0.4353	3.0990	0.17542	3.0953	0.05559	2.1605	-0.2818	1.1129	0.1258	1.1715	-0.1734	1.1109	-0.05339
10	2.1640	-0.1213	3.0929	-0.02387	3.0933	-0.01049	2.1654	-0.05637	1.1116	0.00963	1.1742	0.05551	1.1123	0.07541
12	2.1675	0.04162	3.0937	0.001874	3.0941	0.01520	2.1666	-	1.1112	-0.02359	1.1733	-0.01843	1.1115	-

TABLE 5.3

% Change in the Prototype Element Values due to Rounding of Multiplier Coefficients
Relative BW=1/64

Coefficient Wordlength (Bits)	L_1	% Change	L_3	% Change	L_5	% Change	L_7	% Change	C_2	% Change	C_4	% Change	C_6	% Change
∞	44.1022	-	62.9717	-	62.9717	-	44.1022	-	22.6251	-	23.8871	-	22.6251	-
4	46.5000	5.4370	67.6570	7.4404	67.6570	7.4404	45.5455	3.2726	21.9852	-2.8282	21.9852	-7.9621	21.9785	-2.8578
6	44.0875	-0.03314	63.2773	0.4853	63.2754	0.4823	44.5111	0.9273	22.4842	-0.6227	23.5069	-1.5917	22.478	-0.65
8	43.9362	-0.3762	62.5824	-0.6181	62.5800	-0.6219	44.0110	-0.2067	22.734	0.4815	24.0415	0.6462	22.728	0.4538
10	43.9986	-0.2349	62.8763	-0.1514	62.8740	-0.1551	44.0729	-0.0663	22.6586	0.1479	23.9291	0.1757	22.652	0.1201
12	44.1073	0.01175	62.9717	-	62.9694	-0.00368	44.1039	0.00401	22.6243	-0.0037	23.884	-0.01188	22.6257	0.00247

the manner in which a digital structure is derived. Obviously, for the digital realizations proposed in the 3rd chapter and for Fettweis' new structure, the changes in the element values in the analog reference network due to coefficient rounding are small. Table 5.3 shows the % changes in the analog element values for different coefficient wordlengths. Second, the sensitivity of the analog filter due to element value changes is very low for LC ladder structures. The frequency response of the LC ladder network with element value changes is the same as that of the corresponding wave digital structure with its multiplier coefficients rounded via the bilinear z transform. Hence, the low rms error in the wave digital filters.

5.3 Roundoff Error:

It is difficult to obtain exact analytical expressions for the roundoff error in wave digital filters using floating-point arithmetic, especially when the order of the filter is high. So, an estimate of the roundoff error is obtained by simulation [60].

A seventh-order lowpass Chebyshev filter is considered. Two filter simulations are carried out, one using the full precision of a general purpose computer and the other using a shorter wordlength. In both cases the filter coefficients are represented with full precision. The input and output sequences consist of 2048 samples. The difference in these two output sequences is an estimate of the roundoff error. The sample variances of the ideal output sequence and the error sequence are used as a measure of the average signal and noise power respectively. The signal to noise ratio is calculated for different data wordlengths and relative filter bandwidths. Floating-point rounding is used throughout.

Figs. 5.9, 5.10 and 5.11 show the roundoff noise using a sine wave input sequence with amplitude equal to unity (with frequency equal to 80% of the bandwidth). In Figs. 5.12, 5.13 and 5.14 are shown the signal to noise ratio using white noise input. These figures also show the corresponding quantities for the Fettweis' new structure and the conventional cascade realization [60].

The signal to noise ratio of the conventional cascade form decreases rapidly with decreasing bandwidth whereas it decreases only slightly for the digital structures proposed in the 3rd chapter and for the Fettweis' new structure. For all the three different realizations the signal to noise ratio decreases for decreasing wordlength, as one might expect.

5.4 Conclusions:

In order to assess the suitability of a digital realization for hardware implementation one has to determine the coefficient sensitivity and the roundoff noise associated with the realization. In this chapter we have determined the floating-point coefficient sensitivity and roundoff noise in the wave digital realizations proposed in Chapter 3 and have compared them with those of Fettweis' new structure and the conventional realization [60].

From the coefficient sensitivity found for second-order filters, it is observed that the realization proposed in Chapter 3 has a far better sensitivity than the direct realization and is as good as Fettweis' new structure. A seventh-order Chebyshev lowpass filter is realized in the wave digital form proposed in Chapter 3 and its coefficient sensitivity

computed. It is again found that the sensitivity of this digital structure is far better than that of the conventional form and is comparable to that of Fettweis' new structure.

Roundoff noise in the digital structures proposed in the 3rd chapter is determined by simulating a seventh-order lowpass Chebyshev filter using floating-point arithmetic. The roundoff noise in these structures is compared with those in the conventional cascade form and Fettweis' new structure [60]. It is found that the digital structures proposed in the 3rd chapter give a much lower roundoff noise than the conventional cascade form. For narrow bandwidths it is seen that the wave digital realizations [47] give an improvement of about 45 db over the conventional cascade form. The result obtained is in agreement with Fettweis' theoretical study [59], based on sinusoidal inputs, indicating that digital filters exhibiting lower sensitivity have less roundoff noise.

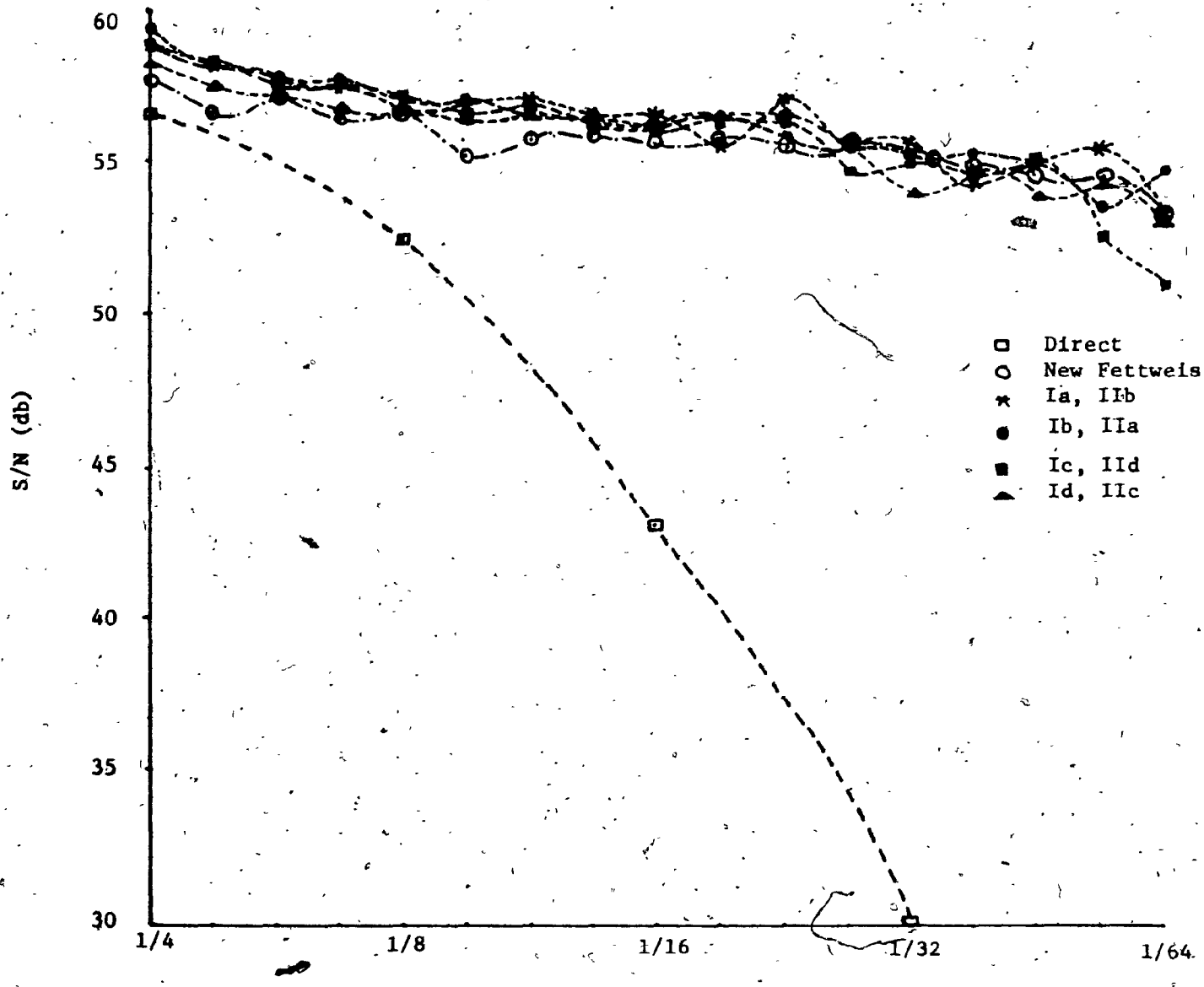


FIG. 5.9 - Roundoff Noise versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Word-lengths of 12 bits with Sinusoidal Input Signal.

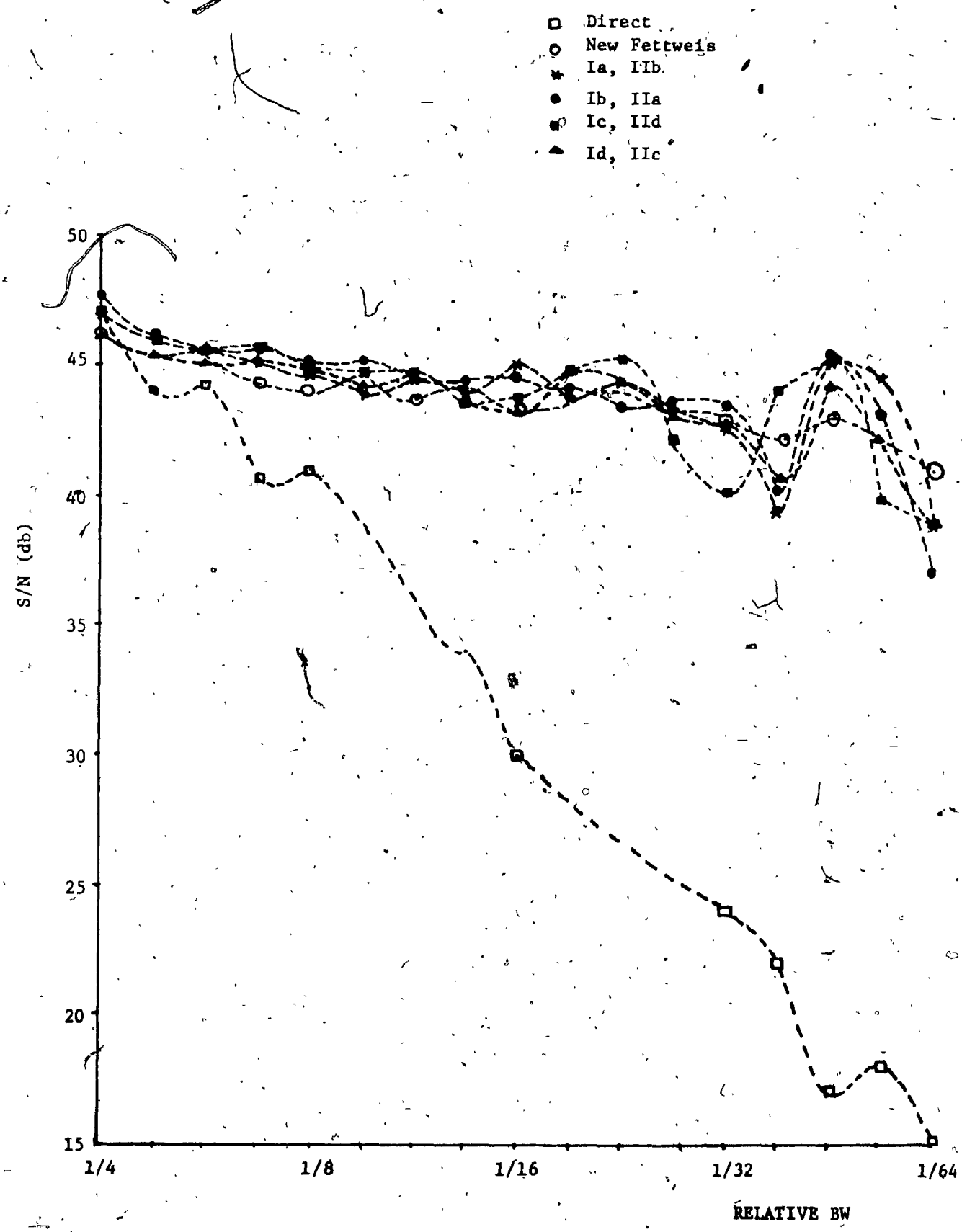


FIG. 5.10 - Roundoff Noise versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Wordlengths of 10 bits with with Sinusoidal Input Signal.

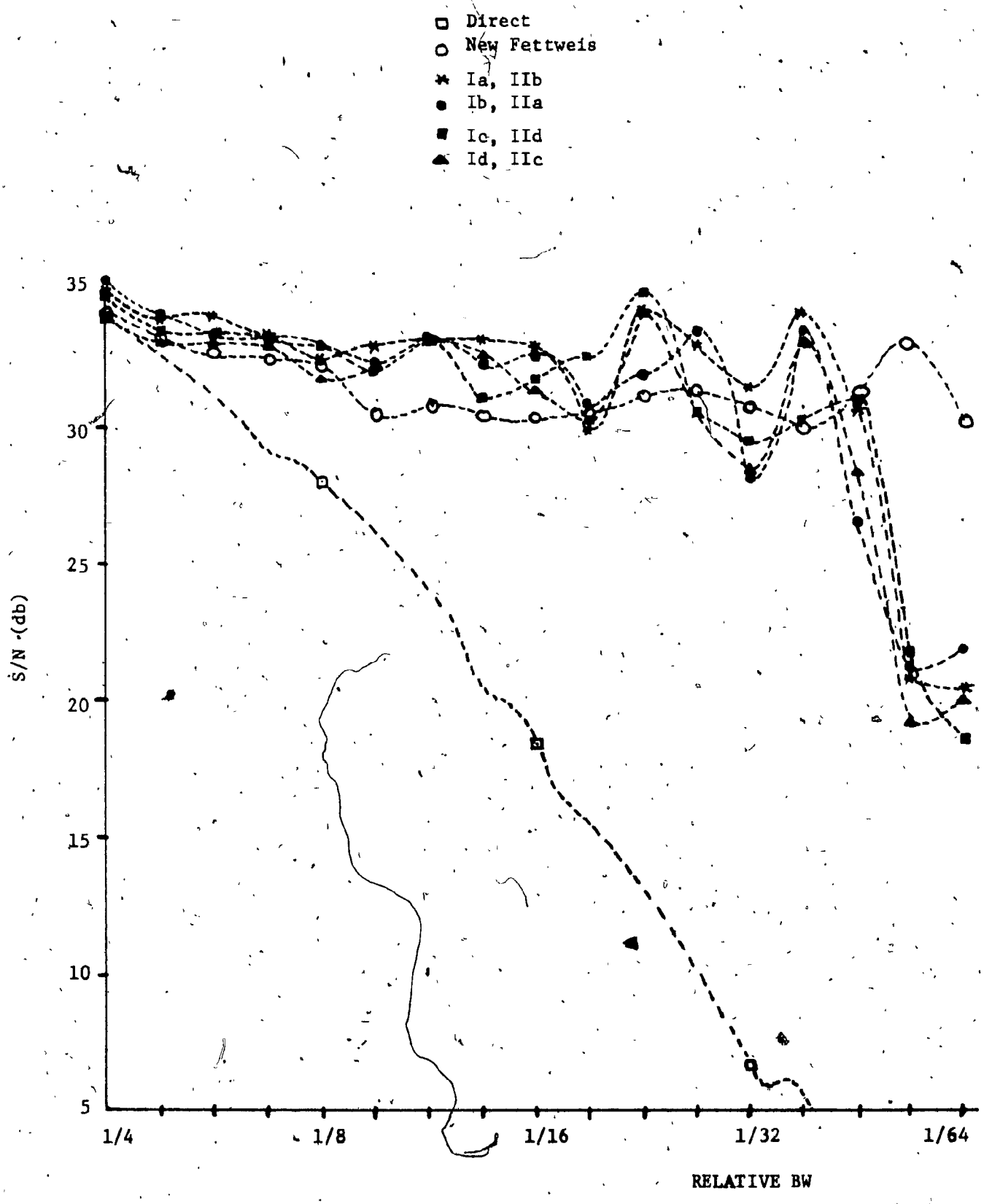


FIG. 5.11 - Roundoff Noise versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Wordlengths of 8 bits with Sinusoidal Input Signal.

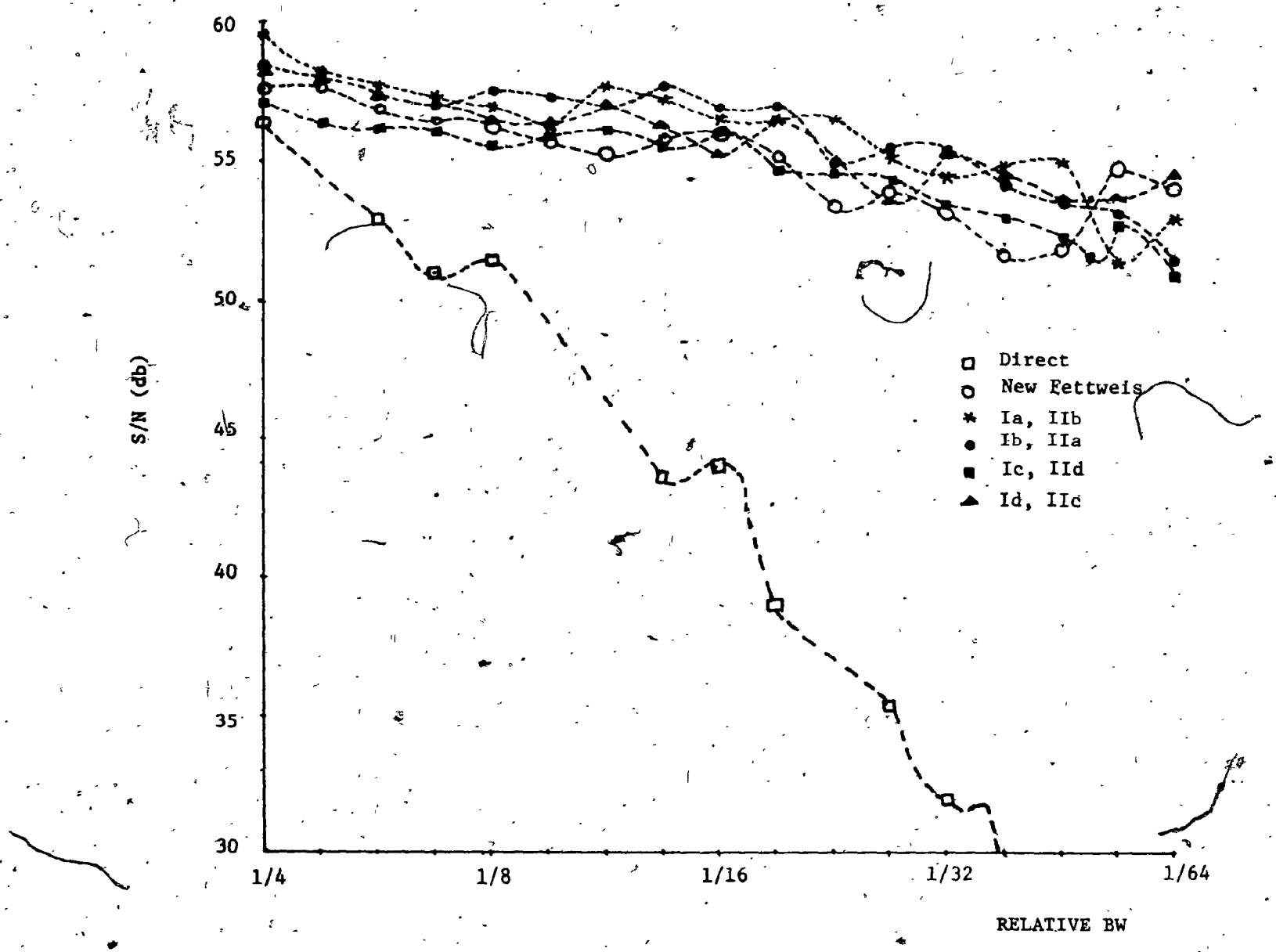


FIG. 5.12 - Roundoff Noise versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Wordlengths of 12 bits with White Noise Input.

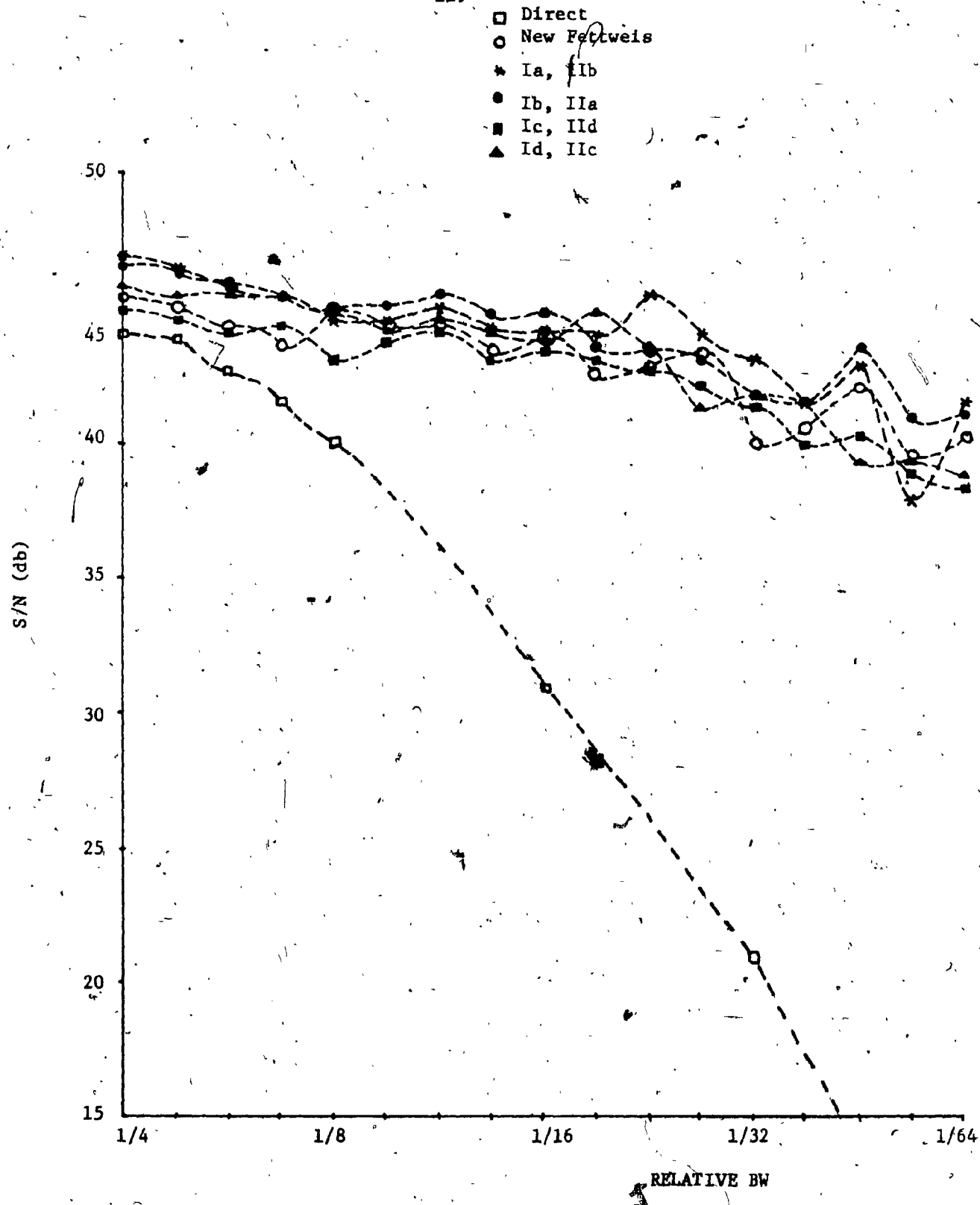


FIG. 5.13 - Roundoff Noise versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Wordlengths of 10 bits with White Noise Input.

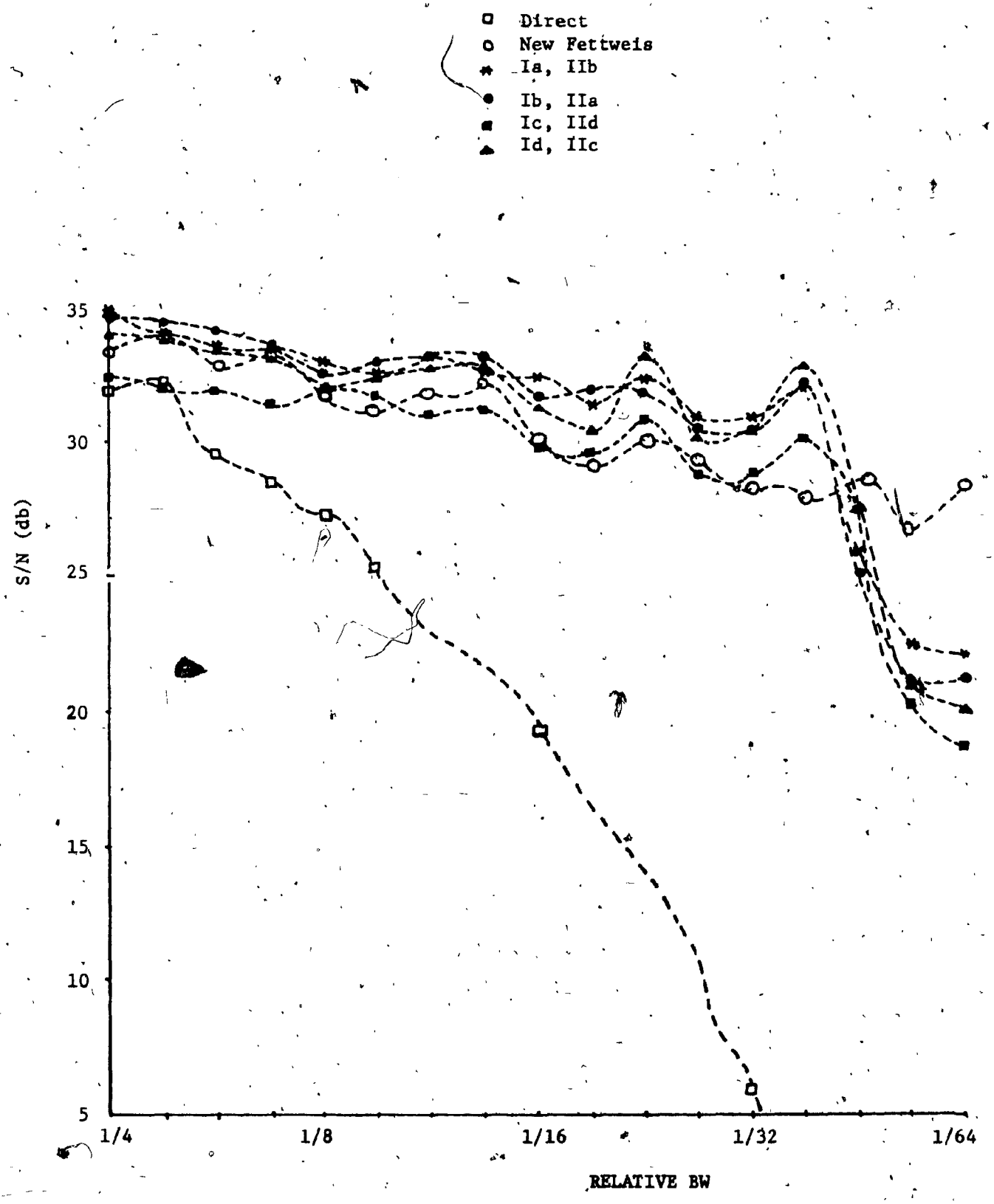


FIG. 5.14 - Roundoff Noise versus Relative Bandwidth for Seventh-order Digital Filters for Coefficient Wordlengths of 8 bits with White Noise Input.

CHAPTER 6

TWO-DIMENSIONAL WAVE DIGITAL FILTERS

6.1 Introduction:

Two-dimensional (2-D) digital filtering has a wide range of applications. For example, areas such as picture processing which includes weather photos, air reconnaissance pictures and medical x-rays and areas where seismic records, magnetic data and electron micrographs are to be processed call for 2-D digital filtering. Therefore, a great deal of attention is currently paid to the development of procedures to synthesize 2-D digital filters.

The major problems involved in 2-D filtering are stability and synthesis. Instability arises in the case of infinite impulse response (IIR) type of 2-D filters while such a problem does not exist in the case of finite impulse response (FIR) type of filters. This is because of the fact that the FIR type has an impulse response sequence which is bounded and of finite duration while that of the IRR type is not of finite duration [32,33]. The IIR type is usually implemented in a recursive fashion and so the corresponding transfer function is a rational polynomial in two variables z_1 and z_2. The stability is, therefore, determined by the zeros of the denominator polynomial of the transfer function. Unlike the one dimensional case, the denominator polynomial of the transfer function of 2-D digital filter may not always be factorable into lower order terms. This introduces difficulties in testing the stability. Even though procedures are available for testing the stability

of 2-D digital filters [35], they are often tedious to use.

There are not many techniques available to synthesize 2-D filters [35-37]. This is partly because not much work has been done in obtaining realizable rational polynomials to approximate specified filter characteristics in the digital domain and partly because of lack of work in that direction in the analog domain. Even the existing synthesis techniques require stability tests which fact is not very encouraging.

Recently it has been reported [43] that 2-D digital transfer function can be obtained to approximate circularly symmetric functions starting with a two-variable passive analog network and then using the double bilinear z transformation $\frac{z_1^{-1}}{z_1+1}$ and $\frac{z_2^{-1}}{z_2+1}$. Such a technique guarantees stability since the analog counterpart is absolutely stable.

But, so far not much attention has been paid to realization techniques [44]. The purpose of this Chapter is to extend the realization procedure discussed in Chapter 3 to 2-D digital filters. Starting with a doubly terminated lossless ladder network in two variables, each of the series and shunt arm elements will be replaced by the corresponding wave digital two-ports and the individual two-ports cascaded to realize the given transfer function in z_1 and z_2. It is expected that, just as the one dimensional wave digital filter derived from a doubly terminated lossless ladder network has excellent sensitivity properties [13,21-28, 46,61] the 2-D digital filter derived from a doubly terminated two-variable LC ladder will also have low sensitivities associated with finite word length of coefficients. That this is so is demonstrated by an example in Section 6.6.

6.2 Two-Dimensional IIR Digital Filters:

A linear time-invariant causal 2-D IIR digital filter is characterized by the 2-D z transform

$$H(z_1,z_2) = \frac{N(z_1,z_2)}{D(z_1,z_2)} = \frac{\sum_{i=o}^{R}\sum_{j=o}^{S} a_{ij} z_1^{-i} z_2^{-j}}{\sum_{i=o}^{R}\sum_{j=o}^{S} b_{ij} z_1^{-i} z_2^{-j}} \qquad (6.1)$$

where $b_{oo}=1$ and a_{ij} and b_{ij} are constant coefficients. The stability, in the bounded-input bounded-output sense, of the 2-D filter is guaranteed iff there exist no values of z_1 and z_2 for which $D(z_1,z_2) = 0$ for $|z_1|$ and $|z_2| \leq 1$ simultaneously [35].

The design of a 2-D IIR digital filter consists of the choice of a_{ij} and b_{ij} in (6.1) such that $H(e^{j\omega_1 T}, e^{j\omega_2 T})$ approximates a given frequency response $H(j\omega_1, j\omega_2)$, where ω_1 and ω_2 are respectively, the horizontal and vertical spatial frequencies. Once the coefficients in (6.1) are found it is necessary to ensure the stability of the filter. If unstable, it has to be stabilized without perturbing the magnitude of its frequency response [35,55].

When we start with a passive analog transfer function and then obtain a corresponding digital transfer function by using the double bilinear z transform, then the stability in the digital domain is guaranteed. This is the approach used in this chapter. The IIR filter design is carried out by first considering a proper two-variable analog passive network to suit the desired frequency specifications. Then, using the double bi-

linear z transform on the transfer function of the chosen network, we can obtain the desired digital transfer function.

6.3 Characterization of a 2-D Wave Digital Two-port:

Consider Fig. 6.1, where the black box $\tilde{N}$ may contain an interconnection of linear elements in two variables p_1 and p_2. Define the wave variables $(\tilde{a}_i, \tilde{b}_i)$, $i=1,2$ by

$$\begin{bmatrix} \tilde{a}_i \\ \tilde{b}_i \end{bmatrix} = \begin{bmatrix} 1 & R_1 \\ 1 & -R_1 \end{bmatrix} \begin{bmatrix} V_i \\ I_i \end{bmatrix} \tag{6.2}$$

where R_1 and R_2 are arbitrary port normalization constants at ports 1 and 2 of $\tilde{N}$. Then we can express $(\tilde{a}_1, \tilde{b}_1)$ in terms of $(\tilde{b}_2, \tilde{a}_2)$ as

$$\begin{bmatrix} \tilde{a}_1 \\ \tilde{b}_1 \end{bmatrix} = \begin{bmatrix} \tilde{\mu} & \tilde{\lambda} \\ \tilde{\nu} & \tilde{k} \end{bmatrix} \begin{bmatrix} \tilde{b}_2 \\ \tilde{a}_2 \end{bmatrix} = [F] \begin{bmatrix} \tilde{b}_2 \\ \tilde{a}_2 \end{bmatrix} \tag{6.3}$$

where

$$\begin{aligned} \tilde{\mu} &= \frac{A+R_1C}{2} + \frac{B+R_1D}{2R_2} \\ \tilde{\lambda} &= \frac{A+R_1C}{2} - \frac{B+R_1D}{2R_2} \\ \tilde{\nu} &= \frac{A-R_1C}{2} + \frac{B-R_1D}{2R_2} \\ \tilde{k} &= \frac{A-R_1C}{2} - \frac{B-R_1D}{2R_2} \end{aligned} \tag{6.4}$$

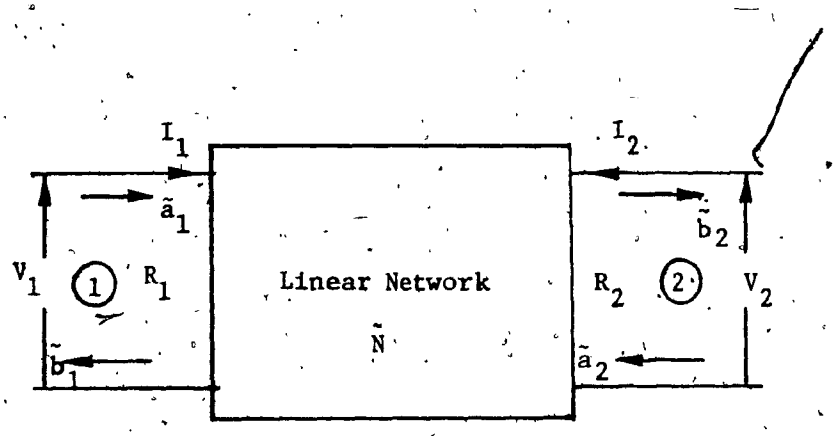


FIG.6.1 - An analog 2-port $\tilde{N}$ containing an interconnection of linear elements in two variables.

and

$$[a] = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \text{Chain matrix of } \tilde{N} \qquad (6.5)$$

It may be observed that the determinant of $[\tilde{F}]$ is,

$$|\tilde{F}| = \frac{R_1}{R_2}(AD-BC) \qquad (6.6)$$

In general, the elements of $[\tilde{F}]$ are functions of p_1 and p_2. If we now use the double bilinear transformation

$$p_i = \frac{z_i - 1}{z_i + 1}, \quad i=1,2 \qquad (6.7)$$

and identify $\tilde{a}_1$ and $\tilde{a}_2$ with the 2-D inputs and $\tilde{b}_1$ and $\tilde{b}_2$ with the 2-D outputs and of a digital filter, then we may recognize (6.3) as the chain matrix description of a 2-D digital two-port. We shall write (6.3) with (6.7) substituted as,

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} \mu & \lambda \\ \nu & k \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} = [F] \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \qquad (6.8a)$$

where

$$[F] = [\tilde{F}] \text{ with } p_i = \frac{z_i - 1}{z_i + 1}, \; i=1,2 \qquad (6.8b)$$

If $\tilde{N}$ is reciprocal, it is seen from (6.6) and (6.8) that

$$|F| = \frac{R_1}{R_2} \tag{6.9}$$

Thus, given any two-variable two-port $\tilde{N}$ with port resistances R_1 and R_2, we may describe a corresponding 2-D wave digital two-port N, whose chain matrix is given by (6.8). It is clear that if $\tilde{N}$ is a cascade of 2-ports, say, $\tilde{N}_1, \tilde{N}_2, \ldots, \tilde{N}_m$, then the corresponding digital two-port is a cascade of the digital two-ports $N_1, N_2, \ldots, N_m$ where N_i is the 2-D digital two-port corresponding to $\tilde{N}_i$; of course, it is assumed that the output-port resistance of $\tilde{N}_i$ is the same as the input port resistance of $\tilde{N}_{i+1}$.

6.4 Realization of the 2-D Digital Two-port:

Consider now the realization of a 2-D digital two-port starting with a two-variable doubly terminated lossless two-port $\tilde{N}$ (Fig. 6.2). From the results obtained in Chapter 3, we have

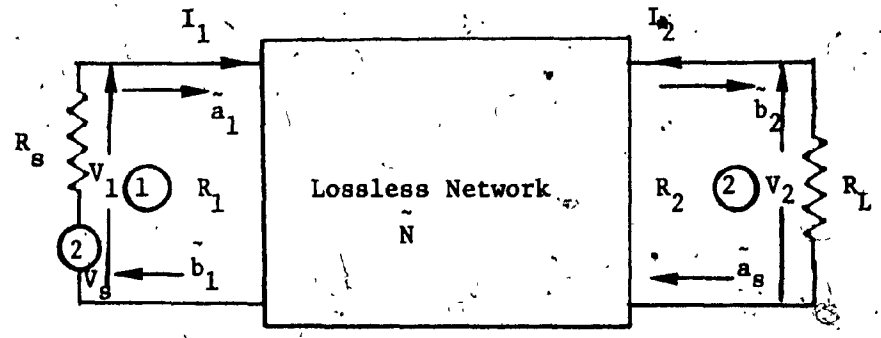
$$\frac{b_2}{a_s} = \frac{2}{1+\phi} \; H(z_1,z_2) \tag{6.10}$$

where

$$H(z_1,z_2) \triangleq \frac{V_2}{V_s}\Bigg|_{p_i=(z_i-1)/(z_i+1),\; i=1,2}$$

$$\phi = (R_L-R_2)/(R_L+R_2)$$

or



$$T(p_1, p_2) = \frac{V_2}{V_s}$$

FIG. 6.2 - A doubly terminated analog 2-port in two variables.

$$\frac{b_2}{a_s} = \frac{1+\theta}{\mu+\lambda\theta+\nu\theta+k\theta\phi} \qquad (6.11)$$

where

$$\theta = (R_1-R_s)/(R_1+R_s)$$

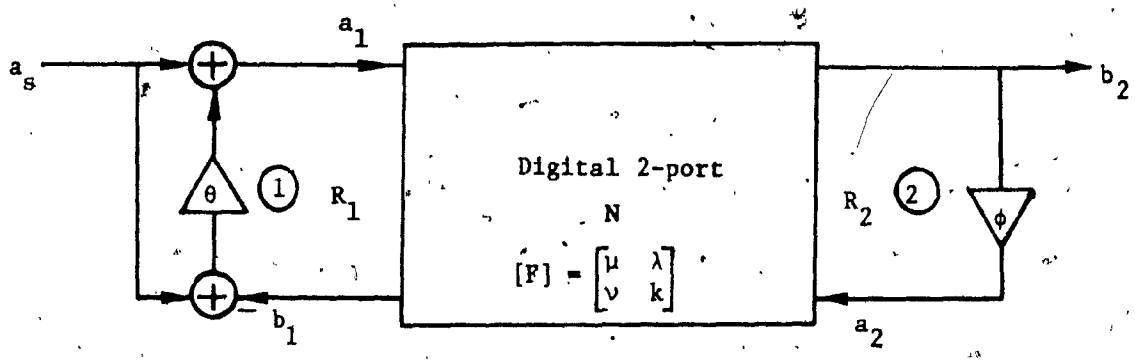
and μ, λ, ν and k are the elements of the chain matrix of the 2-D wave digital two-port N. The corresponding realization is shown in Fig. 6.3, where N is the digital two-port corresponding to $\tilde{N}$.

Thus, given the realization for $T(p_1,p_2) = \frac{V_2}{V_s}$ as a doubly terminated lossless two-port $\tilde{N}$, we can obtain the corresponding realization for $H(z_1,z_2) = \frac{V_2}{V_s}$ with $p_i = (z_i-1)/(z_i+1)$, $i=1,2$ by using Fig. 6.3, where the digital two-port N is obtained from the corresponding lossless two-port $\tilde{N}$.

So far, we have not made any assumptions about $\tilde{N}$. However, in order to realize N from $\tilde{N}$ in a simple fashion, we shall assume $\tilde{N}$ to be a lossless ladder containing elements in two variables p_1 and p_2. Then some of the possible series and shunt arm elements are as shown in Tables 6.1 and 6.2. It is necessary to derive the realizations for the digital two-ports corresponding to these elements which we shall do in the following section. Then, we can cascade them to form N and use Fig. 6.3 to realize $H(z_1,z_2)$.

6.5 Canonic Realization of 2-D Wave Digital Two-ports:

In Chapter 3 we showed that by relaxing the condition $R_1=R_2$,



$$\theta = \frac{R_1 - R_s}{R_1 + R_s} \quad , \quad \phi = \frac{R_L - R_2}{R_L + R_2}$$

$$\frac{b_2}{a_s} = \frac{2}{1+\phi} H(z_1, z_2) \quad , \quad H(z_1, z_2) \triangleq \frac{V_2}{V_s} \text{ with } p_1 = \frac{z_i - 1}{z_i + 1} \quad , \quad i = 1, 2$$

$$a_s = v_s$$

FIG.6.3 - A wave digital 2-port corresponding to the network of Fig. 6.2.

one might obtain a one-dimensional wave digital two-port which is canonic and that there would be no delay-free loops when such two-ports were cascaded.

Following this procedure one can obtain the canonic realizations corresponding to the different series and shunt arm elements in a two-variable ladder network. To this end we start with the series arm elements. When the series arm consists of an L or a C or a parallel combination of an L and a C in one variable, then the corresponding digital two-port is the same as that of the corresponding one given in Chapter 3 with z^{-1} having replaced by z_1^{-1} or z_2^{-1} as the case may be. This is shown in Table 6.1. Next, we shall obtain a realization for the 2-D digital two-port corresponding to the series arm element consisting of L's of p_1 and p_2 types in parallel. This may be done in a simple manner as follows: The impedance of this circuit is

$$Z_s = \frac{1}{1/(L_1 p_1)+1/(L_2 p_2)} \tag{6.12}$$

and

$$Z_1 = Z_s \Big|_{p_i=(1-z_i^{-1})/(1+z_i^{-1}),\ i=1,2}$$

$$= \frac{1}{\frac{1}{L_1}\left(\frac{1+z_1^{-1}}{1-z_1^{-1}}\right) + \frac{1}{L_2}\left(\frac{1+z_2^{-1}}{1-z_2^{-1}}\right)} \tag{6.13}$$

Equation (6.13) may be rearranged in the form

$$Z_1 = \left(\frac{L_1 L_2}{L_1+L_2}\right) \frac{1-\left\{\dfrac{\alpha z_1^{-1}+(1-\alpha) z_2^{-1}-z_1^{-1}z_2^{-1}}{1+(\alpha-1)z_1^{-1}-\alpha z_2^{-1}}\right\}}{1+\left\{\dfrac{\alpha z_1^{-1}+(1-\alpha) z_2^{-1}-z_1^{-1}z_2^{-1}}{1+(\alpha-1)z_1^{-1}-\alpha z_2^{-1}}\right\}} \qquad (6.14)$$

where

$$\alpha = \frac{L_2}{L_1+L_2} \qquad (6.15)$$

Now compare Z_1 in (6.14) with that of an inductor L in one variable in the series arm, namely,

$$Z_1 = L\,\frac{1-z^{-1}}{1+z^{-1}}$$

We then see that an 'L in the one-dimensional case is replaced by $L_1L_2/(L_1+L_2)$ in the 2-D case and z^{-1} by $g(z_1^{-1},z_2^{-1})$ where

$$g(z_1^{-1}, z_2^{-1}) = \frac{\alpha z_1^{-1}+(1-\alpha) z_2^{-1}-z_1^{-1}z_2^{-1}}{1+(\alpha-1)z_1^{-1}-\alpha z_2^{-1}} \qquad (6.16)$$

and α is given by (6.15). The port normalization constants are then related by (from Table 3.2)

$$R_1 = R_2 + \frac{L_1 L_2}{L_1+L_2} \qquad (6.17)$$

Therefore, a realization for this series impedance is obtained by simply replacing z^{-1} in the one-dimensional case corresponding to a series L by $g(z_1^{-1}, z_2^{-1})$ as given in (6.16) with $\sigma=R_2/R_1$ and α as given by (6.15). A realization for $g(z_1^{-1},z_2^{-1})$ in (6.16) is shown in Fig. 6.4, and the corresponding 2-D digital two-port is given in Table 6.1. The realizations for the other series arm configurations, namely, an L of p_1 and a C of p_2 types in parallel and a C of p_1 and a C of p_2 types in parallel, may be obtained merely by replacing z^{-1} in the one-dimensional realization corresponding to an L in the series arm by $g(z_1^{-1}, -z_2^{-1})$ and $g(-z_1^{-1}, -z_2^{-1})$ respectively, where $g(z_1^{-1},z_2^{-1})$ is given by (6.16). In a similar manner, the digital two-ports for the various shunt arm elements may be obtained from the corresponding one-dimensional digital two-ports and are shown in Table 6.2. The realizations in Tables 6.1 and 6.2 are called type Ia realizations. One can also obtain alternate canonic realizations for the series and shunt arm elements in a manner akin to that obtained in Chapter 3. These are called type IIa structures and are shown in Tables 6.3 and 6.4 respectively.

As in the one-dimensional case, one can also derive three more canonic structures corresponding to each of Ia and IIa types. Figs. 6.12a, b and c show the Ib, Ic and Id structures corresponding to Ia type shown in Fig. 6.7. Similarly, one can obtain IIa, IIb, IIc and IId realizations and are shown in Figs. 6.13a, b, c and d respectively.

It should be pointed out here that when using type I structures for the two-dimensional cases, the multiplier ϕ must be set equal to zero or equivalently R_2 must be set equal to R_L in order to avoid a

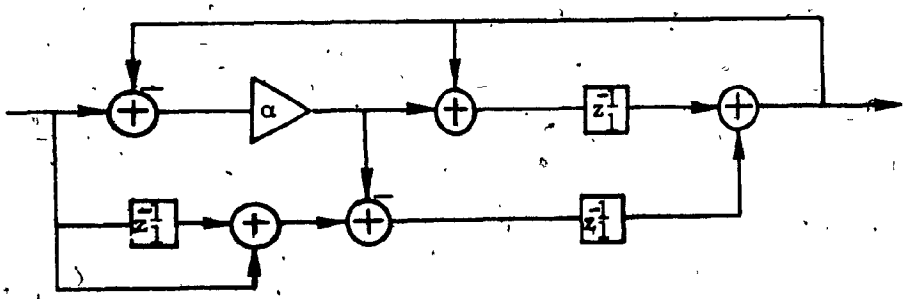


FIG. 6.4 - A digital realization for $g(z_1^{-1}, z_2^{-1})$ of equation (6.16).

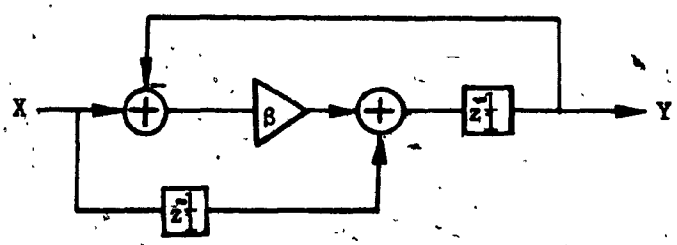
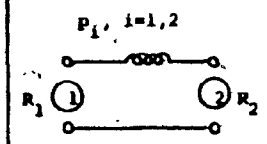
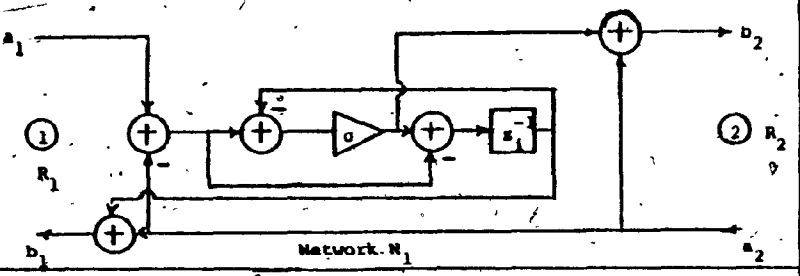
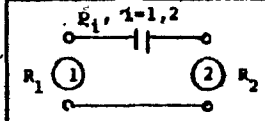
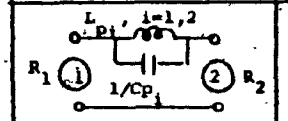
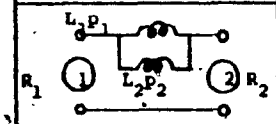
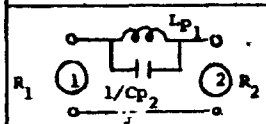
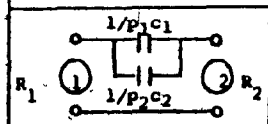


FIG.6.5 - A digital realization for $g_1(z_i^{-1})$ where

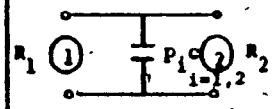
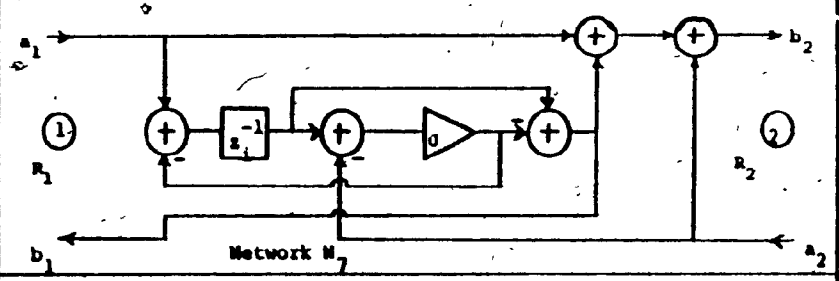
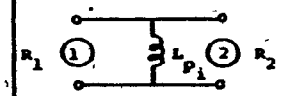
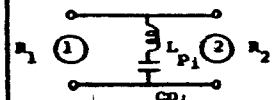
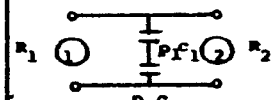
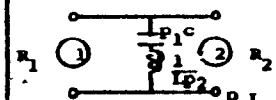
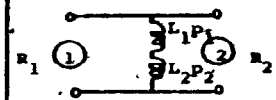
$$\frac{Y}{X} = g_1(z_i^{-1}) = \frac{z_i^{-1}(\beta+z_i^{-1})}{(1+\beta z_i^{-1})}, \quad i=1,2$$

TABLE 6.1

Element	Corresponding Wave Digital 2-port	Relations
	 Network N_1	$\sigma = R_2/R_1$ $R_1 = R_2+L$
	Same as N_1 with z_i^{-1} replaced by $-z_i^{-1}$ Network N_2	$\sigma = R_2/R_1$ $R_1 = R_2+1/C$
	Same as N_1 with z_i^{-1} replaced by $q_1 = \frac{z_i^{-1}(\beta+z_i^{-1})}{1+\beta z_i^{-1}}$ realization for q_1 is shown in Fig. 6.5 Network N_3	$\sigma = R_2/R_1$ $\beta = \frac{1-LC}{1+LC}$ $R_1 = R_2+L/1+LC$
	Same as N_1 with z^{-1} replaced by $g(z_1^{-1}, z_2^{-1})$ as given in eqn. (6.16) Network N_4	$\sigma = R_2/R_1$ $\alpha = \frac{L_2}{L_1+L_2}$ $R_1 = R_2 + \frac{L_1L_2}{L_1+L_2}$
	Same as N_1 with z^{-1} replaced by $g(z_1^{-1}, -z_2^{-1})$ as given in eqn. (6.16) Network N_5	$\sigma = R_2/R_1$ $\alpha = 1/1+LC$ $R_1 = R_2+L/1+LC$
	Same as N_1 with z^{-1} replaced by $g(-z_1^{-1}, -z_2^{-1})$ as given in eqn. (6.16) Network N_6	$\sigma = R_2/R_1$ $\alpha = \frac{C_1}{C_1+C_2}$ $R_1 = R_2 + \frac{1}{C_1+C_2}$

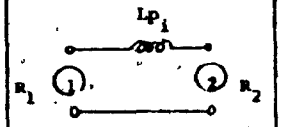
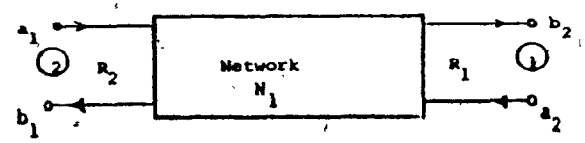
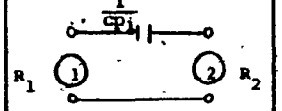
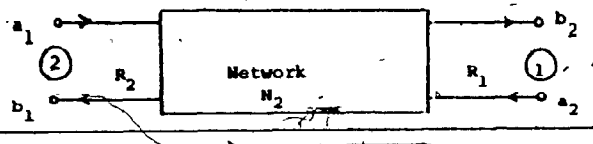
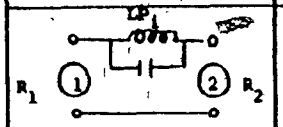
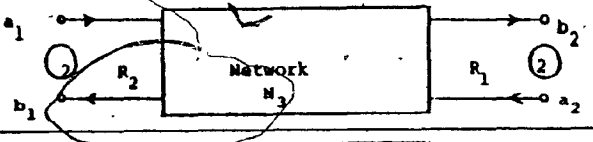
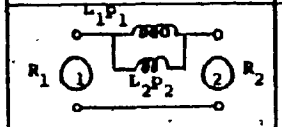
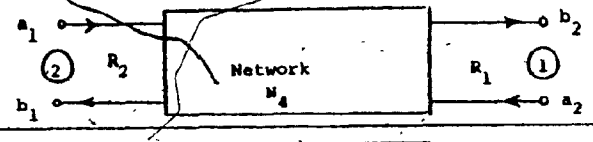
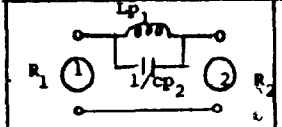
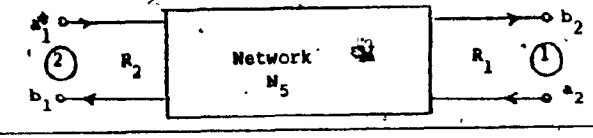
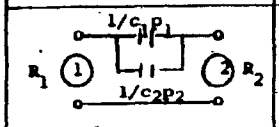
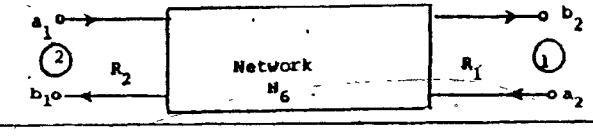
First set of realizations corresponding to the series elements with no delay-free path from a_1 to b_1

TABLE 6.2

Element	Corresponding Wave Digital 2-port	Relations
	 Network N_7	$\alpha = G_2/G_1$ $R_2 = G_1=G_2+C$
	Same as N_7 with z_i^{-1} replaced by $-z_i^{-1}$ Network N_8	$\alpha = G_2/G_1$ $G_1 = G_2+\frac{1}{L}$
	Same as N_7 with z_i^{-1} replaced by $g_1 = \frac{z_i^{-1}(\beta+z_i^{-1})}{1+\beta z_i^{-1}}$ realization for g_1 is shown in Fig. 6.5 Network N_9	$\alpha = G_2/G_1$ $\beta = 1-LC/1+LC$ $G_1=G_2+\frac{C}{1+LC}$
	Same as N_7 with z^{-1} replaced by $g(z_1^{-1}, z_2^{-1})$ as given by eqn. (6.16) Network N_{10}	$\alpha = G_2/G_1$ $\alpha = \frac{C_2}{C_1+C_2}$ $G_1 = G_2 + \frac{C_1C_2}{C_1+C_2}$
	Same as N_7 with z^{-1} replaced by $g(z_1^{-1}, -z_2^{-1})$ as given by eqn. (6.16) Network N_{11}	$\alpha = G_2/G_1$ $\alpha = 1/1+LC$ $G_1 =G_2 + \frac{C}{1+LC}$
	Same as N_7 with z^{-1} replaced by $g(-z_1^{-1}, -z_2^{-1})$ as given by eqn. (6.16) Network N_{12}	$\alpha = G_2/G_1$ $\alpha = L_1/L_1+L_2$ $G_1 = G_2+\frac{1}{L_1+L_2}$

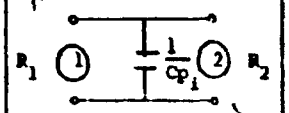
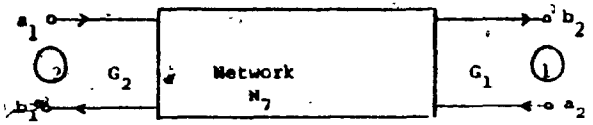
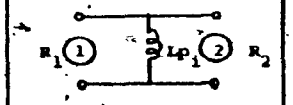
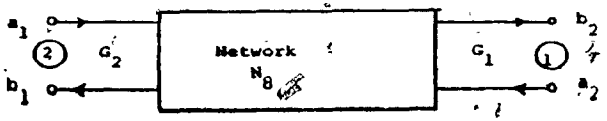
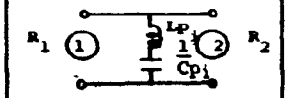
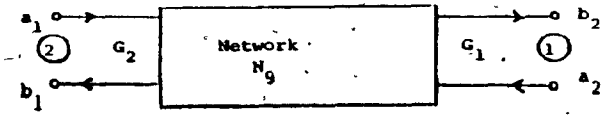
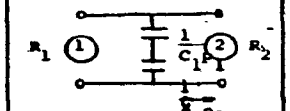
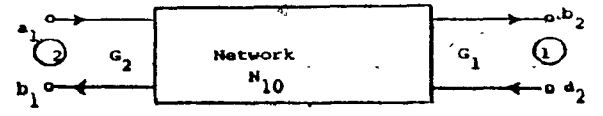
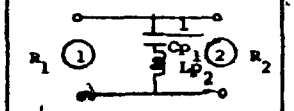
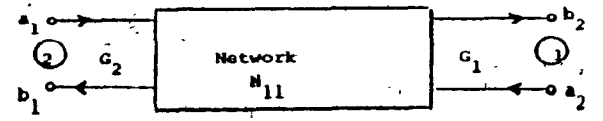
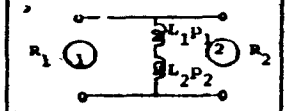
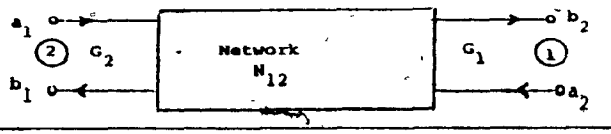
First set of realizations corresponding to the shunt elements with no delay-free path from a_1 to b_1

TABLE 6.3

Element	Corresponding Wave Digital 2-port	Relations
		$\alpha = R_1/R_2$ $R_2 = R_1+L$
		$\alpha = R_1/R_2$ $R_2 = R_1+1/C$
		$\alpha = R_1/R_2$ $\beta = \frac{1-LC}{1+LC}$ $R_2 = R_1 + \frac{L}{1+LC}$
		$\alpha = R_1/R_2$ $\alpha = L_2/L_1+L_2$ $R_2 = R_1 + \frac{L_1 L_2}{L_1+L_2}$
		$\alpha = R_1/R_2$ $\alpha = 1/1+LC$ $R_2 = R_1 + L/1+LC$
		$\alpha = R_1/R_2$ $\alpha = C_1/C_1+C_2$ $R_2 = R_1 + \frac{1}{C_1+C_2}$

Second set of realizations corresponding to the series elements with no delay-free path from a_2 to b_2

TABLE 6.4

Element	Corresponding Wave Digital 2-port	Relations
		$\sigma = G_1/G_2$ $G_2 = G_1+C$
		$\sigma = G_1/G_2$ $G_2 = G_1+\frac{1}{L}$
		$\sigma = G_1/G_2$ $\beta = \frac{1-LC}{1+LC}$ $G_2 = G_1+\frac{C}{1+LC}$
		$\sigma = G_1/G_2$ $\alpha = C_2/C_1+C_2$ $G_2 = G_1+\frac{C_1C_2}{C_1+C_2}$
		$\sigma = G_1/G_2$ $\alpha = 1/1+LC$ $G_2 = G_1+\frac{C}{1+LC}$
		$\sigma = G_1/G_2$ $\alpha = L_1/L_1+L_2$ $G_2 = G_1+\frac{1}{L_1+L_2}$

Second set of realizations corresponding to the shunt elements with no delay-free path from a_2 to b_2

delay-free loop in the overall structure; setting $R_2=R_L$ results in no loss of generality. Similarly, when using type II structures the multiplier θ must be set equal to zero or equivalently R_1 must be set equal to R_s to avoid a delay-free loop; this again results in no loss of generality.

6.6 Design Example:

Let us consider the design of a circularly symmetric IIR 2-D digital filter. It is often necessary, for example in picture processing, to have spatial filters that are insensitive to the relative data orientation.

Since circularly symmetric system functions are not exactly realizable, we may only be able to realize them approximately. Let $\hat{H}(\omega_1,\omega_2)$ be the ideal response in the two spatial frequencies ω_1 and ω_2. Then a suitable analog function $H(\underline{X},\omega_1,\omega_2)$ is chosen to approximate $\hat{H}(\omega_1,\omega_2)$ in a given region, where the vector $\underline{X}$ is the design parameter. Since the transfer function of the 2-D digital filter is periodic in ω_1 and ω_2 with period $\frac{2\pi}{T}$, only values of ω_1 and ω_2 in the region

$$W_1 = \{\omega_1 : -\frac{\pi}{T} \le \omega_1 \le \frac{\pi}{T}\}$$

$$W_2 = \{\omega_2 : -\frac{\pi}{T} \le \omega_2 \le \frac{\pi}{T}\}$$

need be considered. We now define an error function $r(\underline{X}, W_1, W_2)$ to be

$$r(\underset{\sim}{X}, \omega_1,\omega_2) = |\hat{H}(\omega_1,\omega_2)| - |H(\underset{\sim}{X},\omega_1,\omega_2)| \tag{6.18}$$

The approximation then consists in minimizing some norm of $r(\underset{\sim}{X},\omega_1,\omega_2)$ in the region W_1,W_2 subject to $\underset{\sim}{X}$ constrained to a particular region. If the approximating function corresponds to a passive network, then $\underset{\sim}{X}$ represents the element values. Then $\underset{\sim}{X}$ is restricted to take on only positive values. In this example, we will be using minimax error criterion so that the approximation problem lies in minimizing the maximum absolute error, i.e., minimize

$$\max_{\substack{\omega_1 \epsilon W_1 \\ \omega_2 \epsilon W_2}} |r(\underset{\sim}{X}, \omega_1,\omega_2)|$$

such that $\underset{\sim}{X}>0$.

Returning to the design problem in question, when no structure exists a priori, one way is to start with a given order doubly terminated LC ladder in two variables in which each reactive element can be associated with either a p_1 or a p_2 type, as in Fig. 6.6a. Another way [56] is to consider first a given order doubly terminated LC ladder in one variable, say p, and then transform p into $(\alpha_1 p_1+\beta_1 p_2)$. Then, in both cases using minimax error criterion [57] the various L's and C's and the terminating resistor as design parameters, one can approximate the desired spatial frequency response. We shall, however, use the first

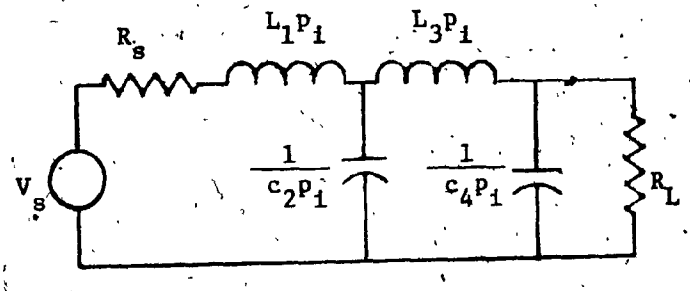


FIG. 6.6a -A two-variable doubly terminated LC ladder, of order 2 in each variable.

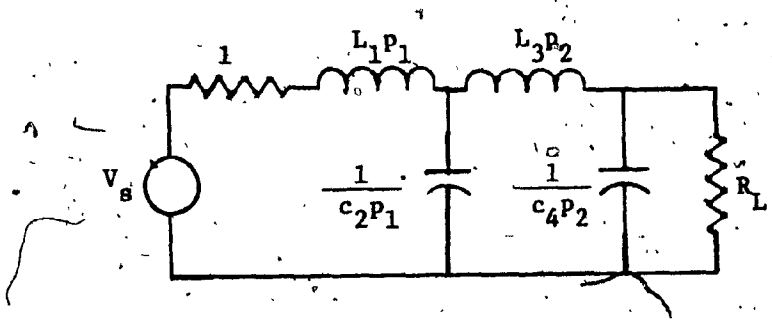


FIG. 6.6b- A two-variable doubly terminated LC ladder in which the p_1 type elements are cascaded with p_2 type elements.

method in the example to follow.

Let us then design a circularly symmetric 2-D digital filter to have pass and stopband edges of $0.14\pi/T$ and $0.26\pi/T$ respectively. This example is taken from Ref. [43]. In Ref. [43] they have found that the approximation was acceptable only when the elements of p_1 type were cascaded with that of p_2 type. So, we select a doubly terminated 4th order LC ladder network of the type shown in Fig. 6.6b. The initial element values of the ladder of Fig. 6.6b correspond to the Butterworth type of response along $p_1 = p_2 = p$. The final parameter values are then obtained using the optimization procedure cited in [57]. The required 2-D digital transfer function is finally obtained from the transfer function of the analog network of Fig. 6.6b using double bilinear z transform, $p_i = \frac{z_i - 1}{z_i + 1}$, $i=1,2$ and is found to be

$$H(z_1,z_2) = \frac{(1/1207.25)(z_1+1)^2\,(z_2+1)^2}{\{z_1^2z_2^2-1.577z_1^2z_2-1.547z_1z_2^2+0.69z_1^2+0.665z_2^2+2.441z_1z_2 -1.067z_1-1.049z_2+0.459\}} \qquad (6.19)$$

Equation (6.19) may be written approximately as

$$H(z_1,z_2) = \frac{(1/1207.25)(z_1+1)^2(z_2+1)^2}{(z_1^2-1.55z_1+0.67)(z_2^2-1.58z_2+0.69)} \qquad (6.20)$$

It is found that the absolute maximum deviation of the actual response from the desired response in the region of interest is somewhat smaller than that obtained in Ref. [43]. Fig. 6.7 shows the digital realization

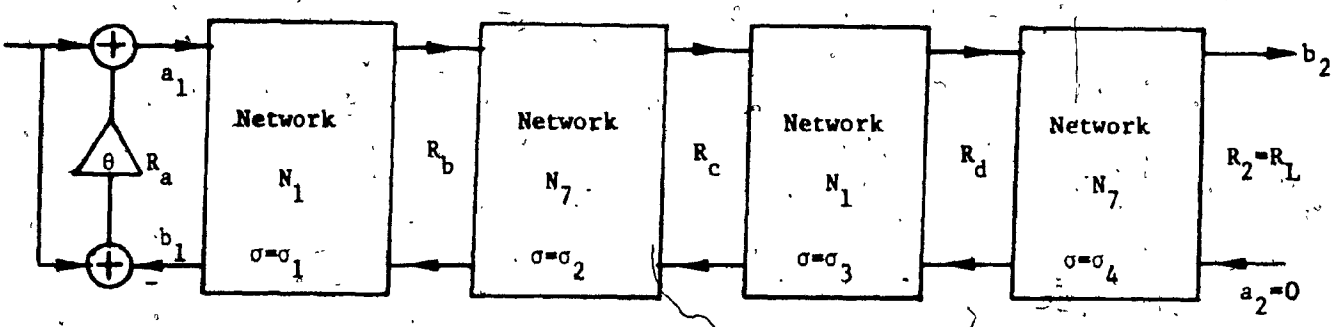


FIG. 6.7 - Type Ia digital realization corresponding to the network of Fig. 6.6b.

corresponding to the network of Fig. 6.6b.

The surface plotting of the frequency response of the 2-D digital filter of Fig. 6.7 is shown in Fig. 6.8, and Fig. 6.9 shows the contour plots of constant magnitude of its transfer function. The contours are displayed in steps of 0.1.

In order to show the good sensitivity properties of 2-D wave digital filters, plots are obtained for the contours for different fixed-point quantization levels of the multipliers of the wave digital filter of Fig. 6.7. These are shown in Fig. 6.10 where one particular contour in the passband is shown. To compare this with the direct realization, the same transfer function in equation (6.20) is realized by the direct method and the corresponding contour plots for different fixed-point quantization levels of the multipliers are shown in Fig. 6.11. Inspection shows that wave digital realization is desirable compared to the direct realization. It is interesting to note that realization is possible in wave digital configuration for the example considered even with 7 bits for multipliers while it is not possible for the direct realization of $H(z_1,z_2)$ in (6.20) even with 10 bits.

6.7 Conclusions:

A low sensitive realization for a 2-D digital filter of the IIR type is given in this chapter. Doubly terminated lossless ladder networks in two variables were considered where the different series and shunt arm elements were characterized by transfer scattering matrices. Using the double bilinear z tranform $p_i = (z_i-1)/(z_i+1)$, i=1,2, each transfer scattering matrix was transformed into a corresponding chain matrix

of a digital two-port with the incident and reflected waves being identified with the digital inputs and outputs respectively, and the individual digital two-ports cascaded to realize the overall chain matrix.

For a given analog ladder structure, eight digital realizations were obtained which were all canonic in multipliers. The sensitivity of one of these digital structure was found to be much better than that of the corresponding direct realization.

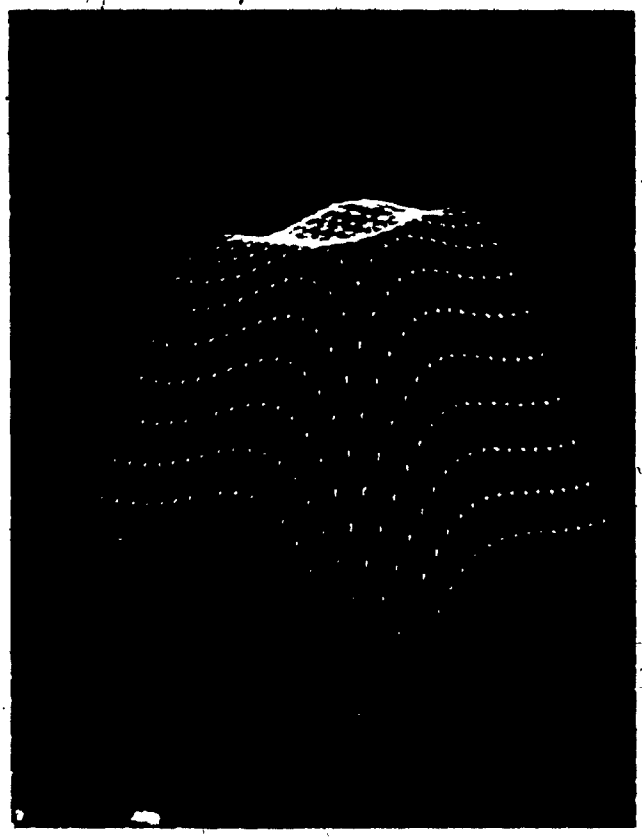


FIG. 6.8 - The surface plotting of the frequency response of the 2-D wave digital filter of Fig. 6.7.

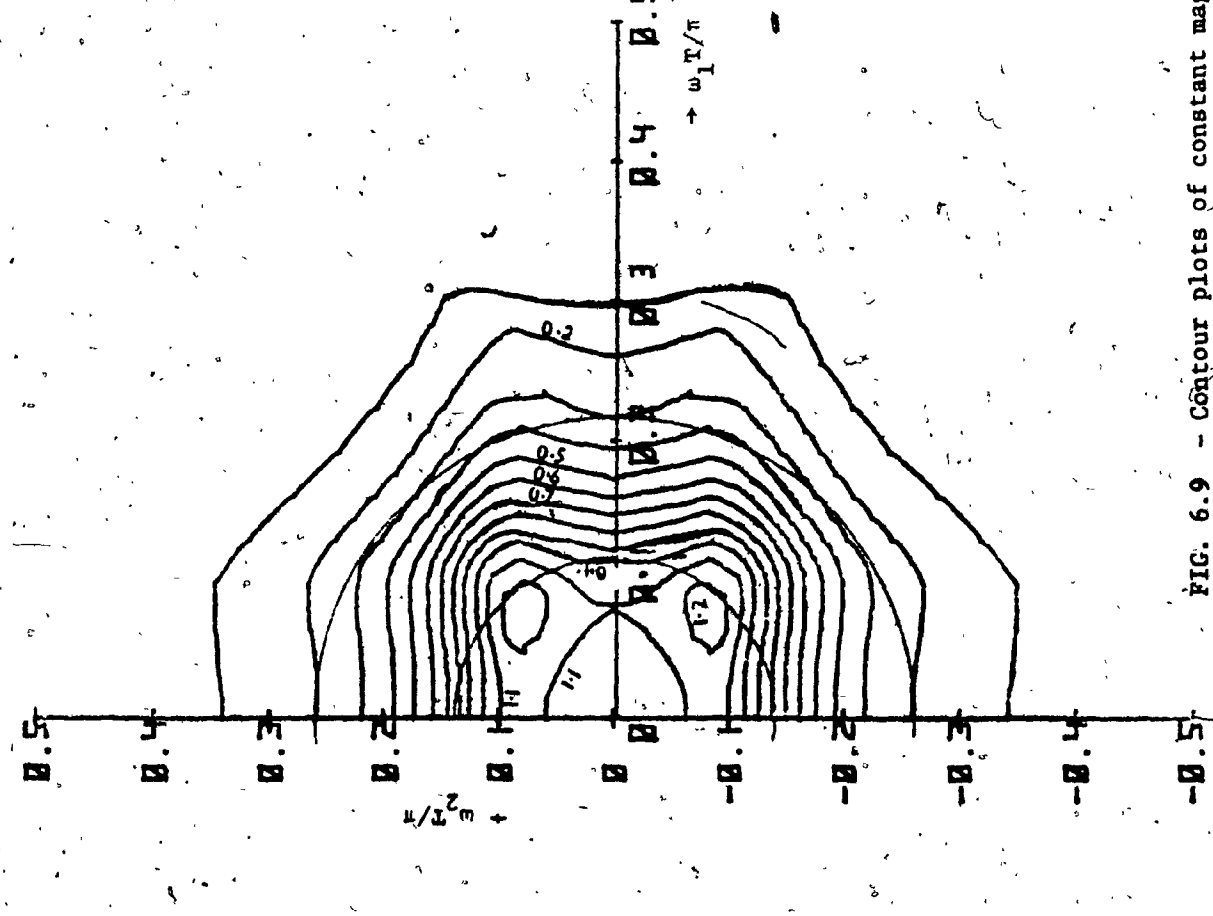


FIG. 6.9 - Contour plots of constant magnitude of the transfer function of the wave digital filter of Fig. 6.7. The contours are displayed in steps of 0.1.

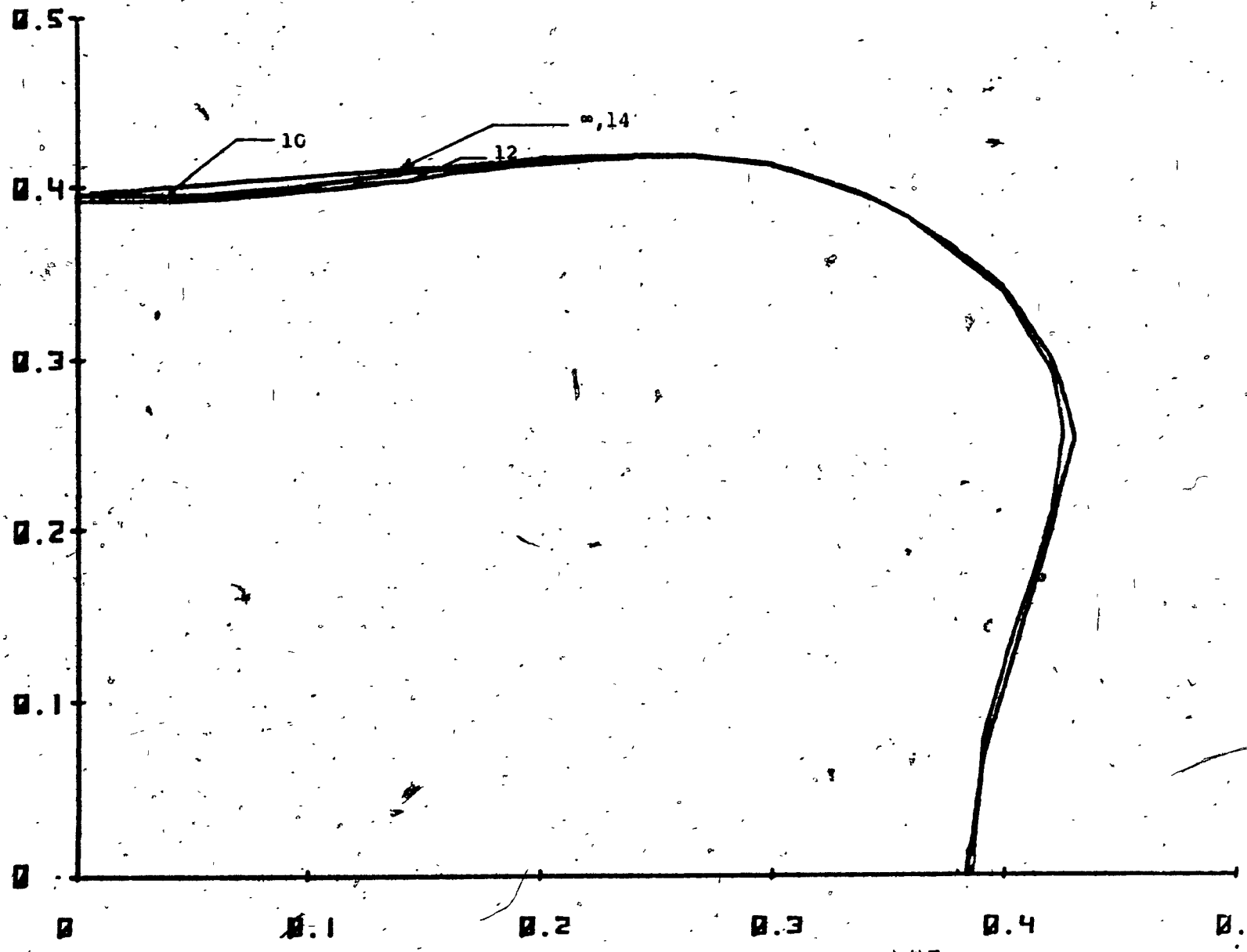


FIG. 6.10 – Plots of the contour for the wave digital filter of Fig. 6.7, corresponding to the magnitude of 0.9 in the passband for different fixed-point quantizations of its multiplier coefficients.

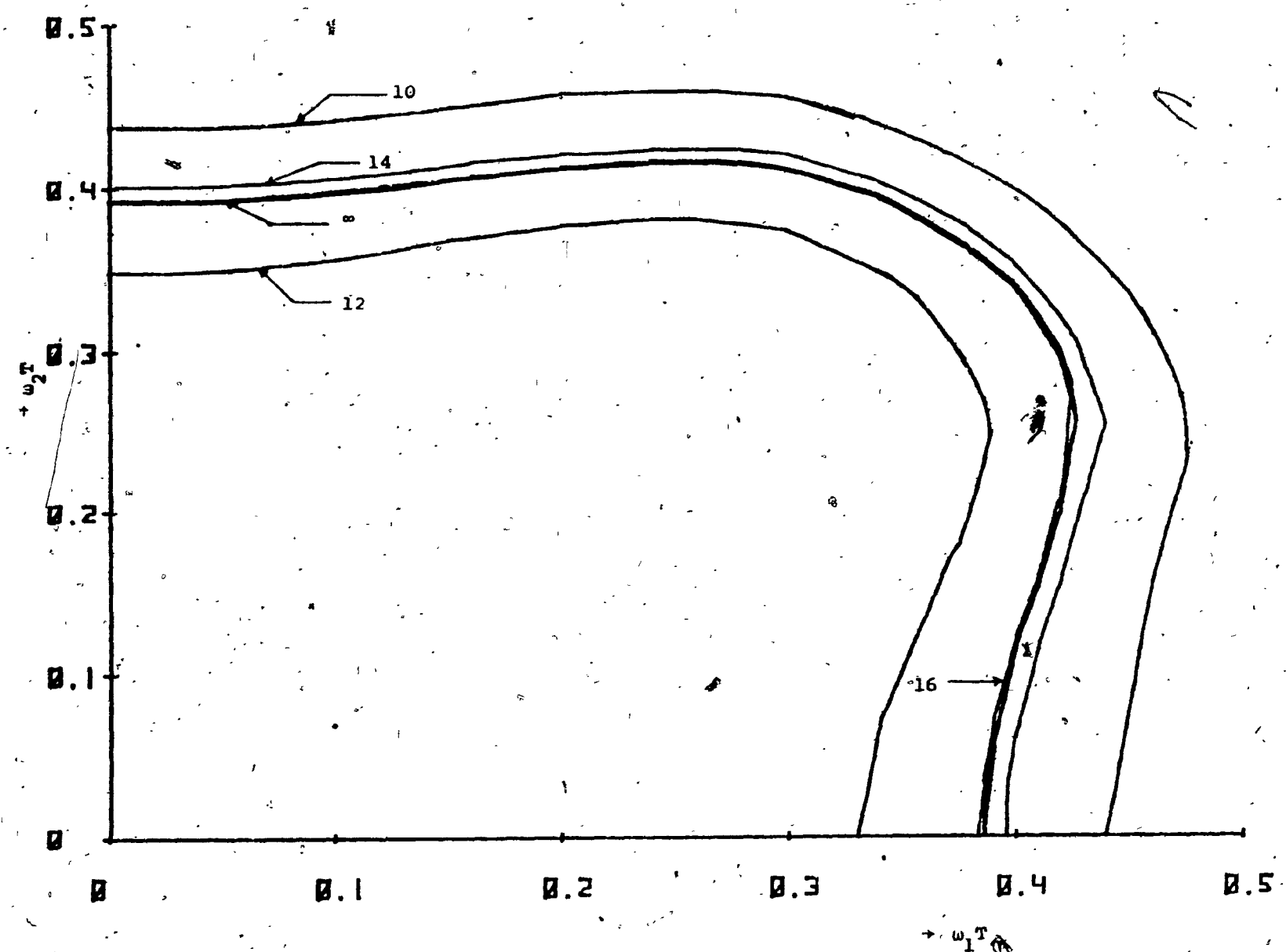
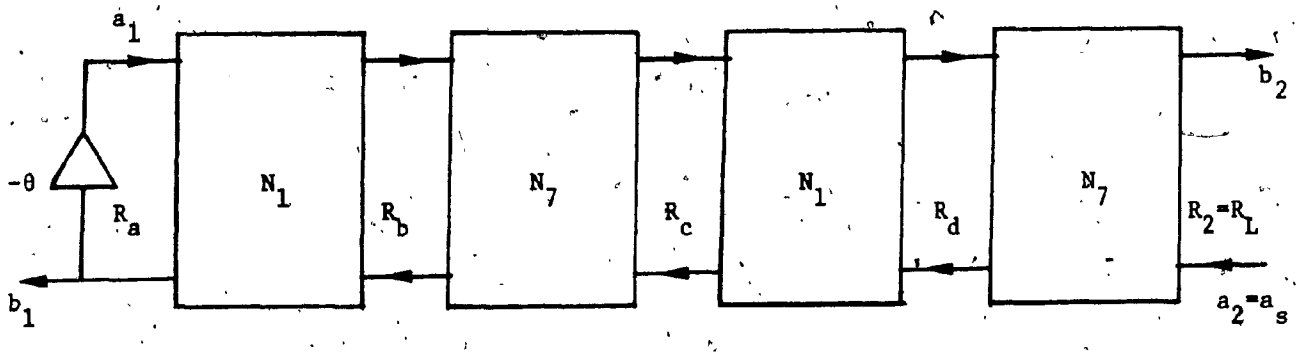
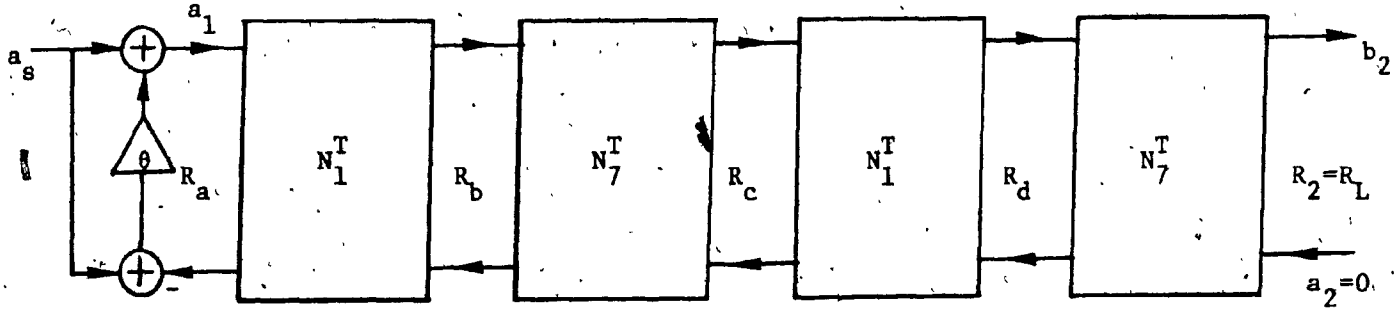


FIG. 6.11 - Plots of the contour for the direct digital realization of equation (6.20) corresponding to the magnitude of 0.9 in the passband for different fixed-point quantizations of its multiplier coefficients.



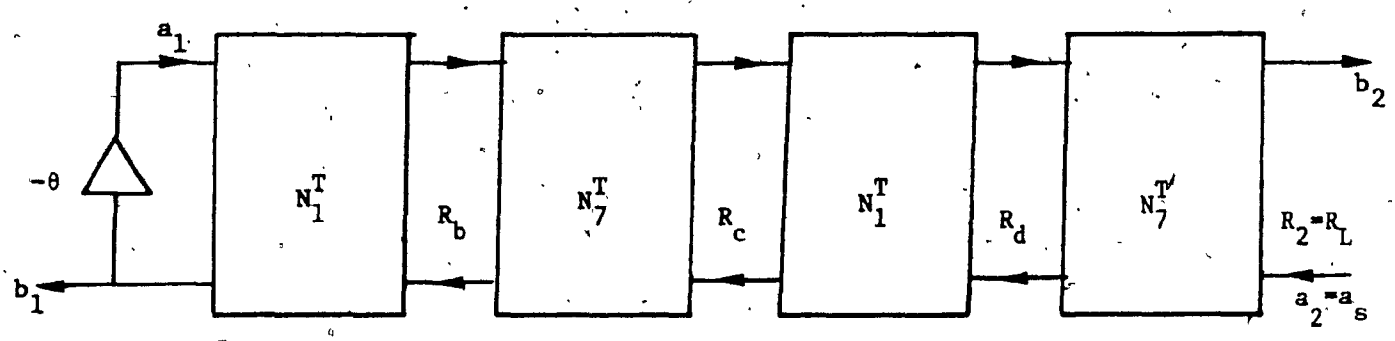
$$\frac{b_1}{a_2} = \frac{R_d}{R_L}\,\frac{1}{1+\theta}\,2\,.\,H(z_1,z_2)\,,\quad a_s=v_s$$

FIG. 6.12a - Type Ib digital realization corresponding to the network of Fig. 6.6b.



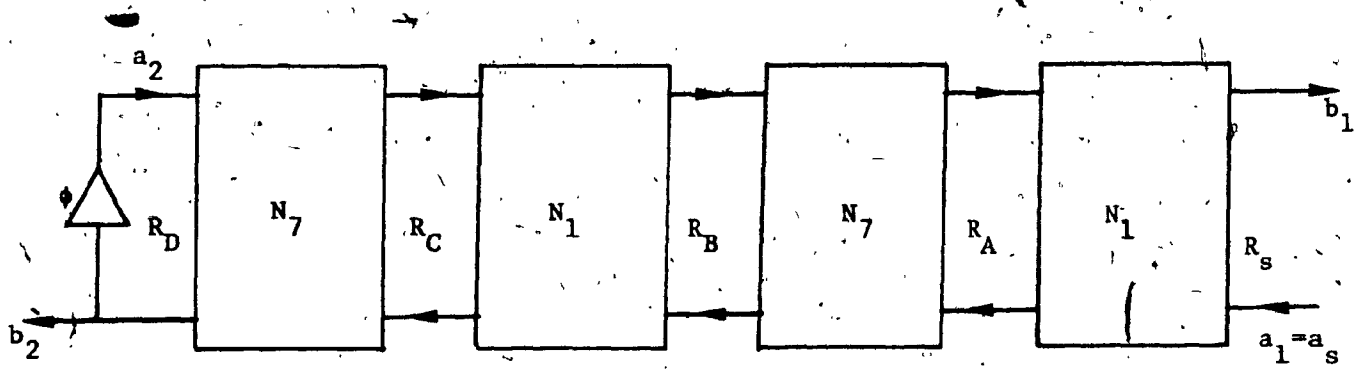
$$\frac{b_2}{a_s} = \frac{R_d}{R_L} \cdot 2\,H(z_1,z_2) \quad , a_s=v_s$$

FIG. 6.12b - Type Ic digital realization corresponding to the network of Fig. 6.6b.



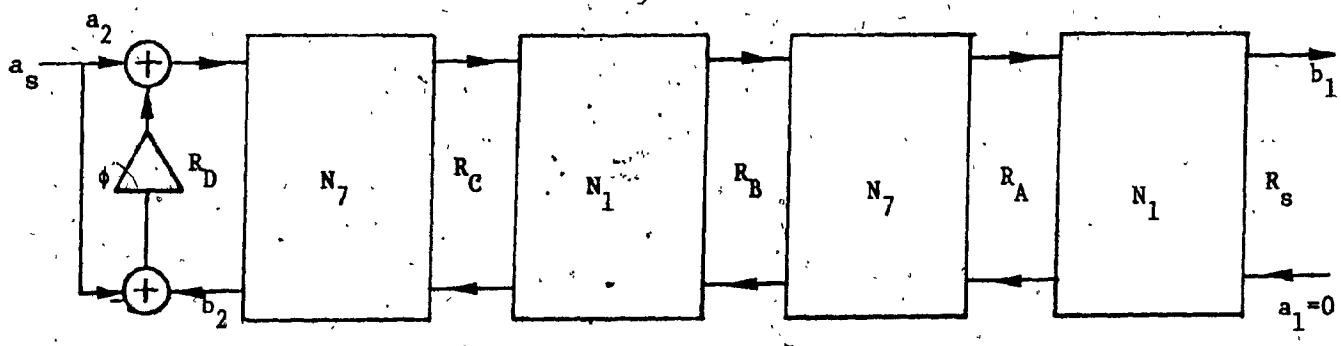
$$\frac{b_1}{a_2} = \frac{2}{1+\theta} H(z_1, z_2) \quad , \; a_s = v_s$$

FIG. 6.12c - Type Id digital realization corresponding to the network of Fig. 6.6b.



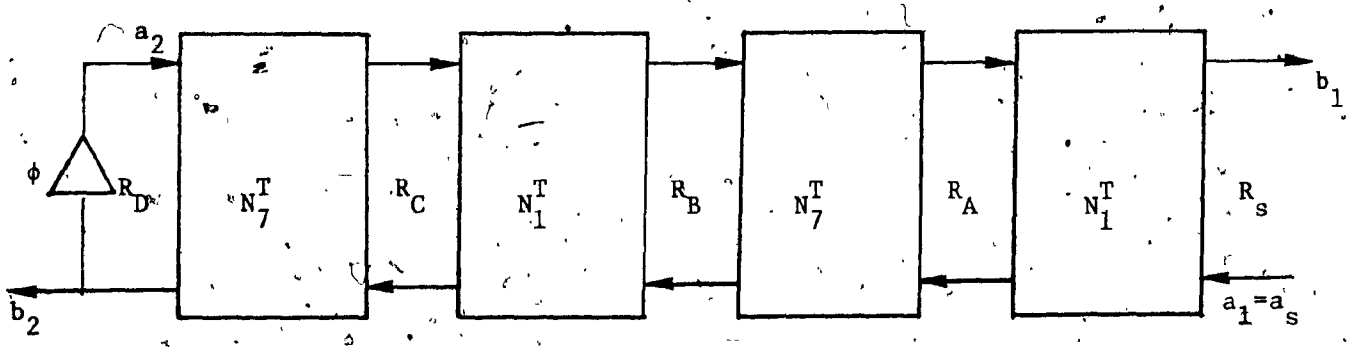
$$\frac{b_2}{a_s} = \frac{2}{1+\phi} \; H(z_1,z_2) \; , \; a_s=v_s$$

FIG. 6.13a - Type IIa digital realization corresponding to the network of Fig. 6.6b.



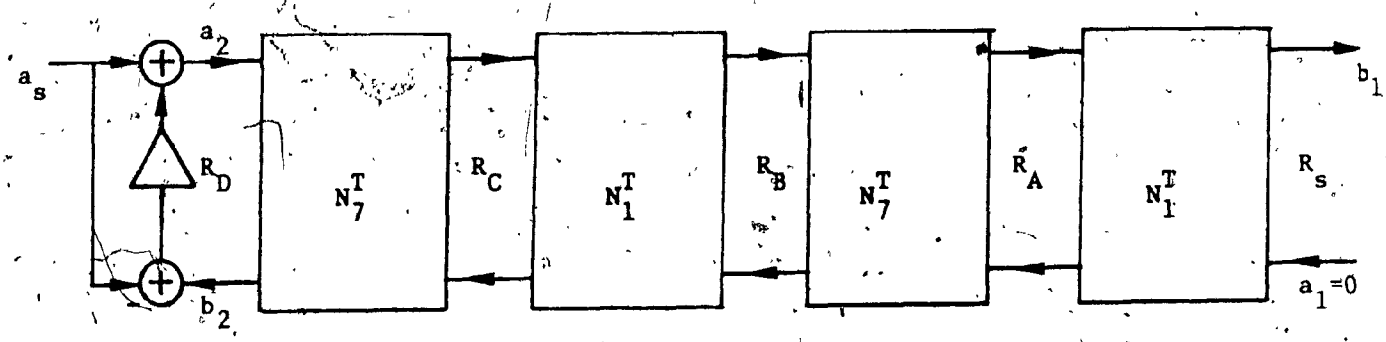
$$\frac{b_1}{a_s} = \left(\frac{R_s}{R_L}\right) 2\, H(z_1, z_2) \quad , \; a_s = v_s$$

FIG. 6.13b - Type IIb digital realization corresponding to the network of FIG. 6.6b.



$$\frac{b_2}{a_s} = \frac{R_s}{R_D} \cdot \frac{2}{1+\phi} \quad H(z_1, z_2) \,, \quad a_s \neq v_s$$

FIG. 6.13c - Type IIc digital realization corresponding to the network of Fig. 6.6b.



$$\frac{b_1}{a_s} = \left(\frac{R_D}{R_L}\right) 2 \cdot H(z_1, z_2) \quad , \quad a_s = v_s$$

FIG. 6.13d - Type IId digital realization corresponding to the network of Fig. 6.6b.

CHAPTER 7

CONCLUSIONS

7.1 Conclusions:

A new type of wave digital filter structure, derived from a doubly terminated lossless network, has been proposed in this Thesis. A linear, lumped, time-invariant, lossless network is first described by a wave or scattering matrix where the incident and reflected waves at the two ports are related to the voltages and currents at the respective ports through the chain parameters of the two-port. Using the bilinear z transform, the wave matrix of the analog network is then transformed into a chain matrix description of a digital two-port where the digital inputs and outputs are identified with the respective incident and reflected waves at the ports of the analog network. A realization is then obtained corresponding to this chain matrix of the digital two-port.

Since LC ladder networks have low sensitivity properties due to element changes [49], specifically, doubly terminated LC ladders have been considered in deriving the wave digital structures. The different possible series elements could only be an L or a C or an LC parallel circuit while the shunt elements could only be an L or a C or an LC series circuit (since any reactance function can always be expressed in Foster's I or II form). Therefore, both canonic and noncanonic digital realizations for these series and shunt elements have been derived. For those realizations which are canonic with respect to the multipliers but not with respect to the delays, all port resistances are assumed equal. This results in a delay-free loop when the digital two-ports

corresponding to the different series and shunt elements of the ladder are cascaded even though the individual two-ports have no delay-free loop in themselves. Therefore, extra delays are introduced between successive digital two-ports for physical realizability condition.

The condition on the port resistances is relaxed for those realizations which are canonic with respect to both the multipliers and delays. A relation between the port resistances is obtained in such a way that there is no delay-free path from the incident to the reflected waves at the input port. This ensures that there be no delay-free loop in the overall digital structure.

For a given analog structure eight different digital structures are obtained, all of them being canonic with respect to both the multipliers and delays.

The floating-point coefficient sensitivity and roundoff noise properties of these digital structures have been studied. For sensitivity analysis an rms value defined in [60] has been used to measure the deviation of the actual frequency response from the ideal one when the multiplier coefficients are rounded for implementation. First a second-order lowpass Butterworth filter is realized in i) the direct form and ii) the proposed wave digital form. Then the rms value so defined is computed for those two digital configurations for the coefficient word lengths of 8 and 12 bits for different relative bandwidths. It is found that the sensitivity of the proposed digital structures is much lower than that of the direct form and is comparable to that of Fettweis' new structure [60]. A similar study is made for a seventh-order Chebyshev filter realized in the proposed

form and in the conventional cascade form. It is again found that the sensitivity of the proposed structures is far better than the conventional cascade realization and comparable to that of Fettweis' new structure [60].

The roundoff noise has been studied by simulating a seventh-order lowpass Chebyshev filter on a digital computer using full precision and shorter word lengths. The difference in the output sequences of these two filters is treated as a measure of the roundoff noise in the filter implemented. The average signal power is proportional to the variance of the input sequence while the average noise power is proportional to the variance of the difference sequence. The signal to noise ratio is calculated for i) the proposed digital structures and ii) the conventional cascade form as a function of the relative bandwidths for the coefficient word lengths of 8, 10 and 12 bits respectively. It has been found that the proposed digital realizations have a high signal to noise ratio as compared to the conventional cascade structure. It has also been found that for all the eight structures proposed, the signal to noise ratio decreases much less rapidly with decreasing relative bandwidth (or increasing sampling frequency) while for the conventional cascade structure it falls off very rapidly. It is further found that the signal to noise ratio of the proposed structure is comparable to that of Fettweis' new structure [60].

Wave digital realizations for bandpass and bandstop filters with variable center frequency and bandwidth have been obtained. Starting with a prototype lowpass wave digital filter it has been shown that a bandpass or a bandstop digital filter could be obtained by first recalculating

the prototype multiplier values corresponding to the required bandwidth and then replacing each delay element in the prototype structure by an appropriate function $g(z^{-1})$. It has also been shown how to obtain $g(z^{-1})$ from the appropriate frequency transformation in the analog domain.

The procedure for the proposed digital realization has been extended to the case of a 2-D digital filter realization. Starting with a doubly terminated LC ladder network in two variables, digital realizations for some of the possible series and shunt elements of the ladder have been derived which are canonic with respect to multipliers. An example of designing a circularly symmetric 2-D digital filter has been considered, where a procedure is outlined as to how to go about choosing a particular network structure and then obtain the element values using a known optimization procedure to approximate the desired spatial frequency response. Contour plots for the magnitude response have been obtained for i) the wave digital realization and ii) for the direct form realizing the same 2-D transfer function. The results show that the 2-D wave digital structure exhibits much lower sensitivity to multiplier coefficient rounding than the direct realization.

7.2 Scope for Further Work:

Further worthwhile investigations could be carried out in the areas of error analysis and digital realizations. Since a digital filter is usually implemented with fixed-point arithmetic, it is necessary to carry out the sensitivity and roundoff noise analysis in fixed-point form for the proposed digital realizations. It is also necessary to investigate the existence of limit cycles in the proposed digital structures

and derive the bounds on such oscillations.

Lattice networks are another class of important analog structures. The proposed wave digital realization procedure may be applied to these lattice networks to obtain a different class of digital networks.

In realizing a circularly symmetric 2-D digital filter we started with a doubly terminated LC ladder in one variable, then assumed that half of the LC elements to be of p_1 type and the remaining half to be of p_2 type. Instead, one can transform each reactive element in the one-variable ladder into a two-variable reactive element, i.e., $p \rightarrow \alpha_i p_1 + \beta_i p_2$ [56], and then carry out the optimization procedure. This may give rise to a better approximation to the ideal circularly symmetric response since there are more number of degrees of freedom.

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